Aranjuez, Spain

FEBRUARY, 11TH - 13TH, 2015

10th Spanish Conference on Electron Devices

evento.es
congresos
y servicios

www.cde2015.es

2015 10th Spanish Conference on Electron Devices (CDE)

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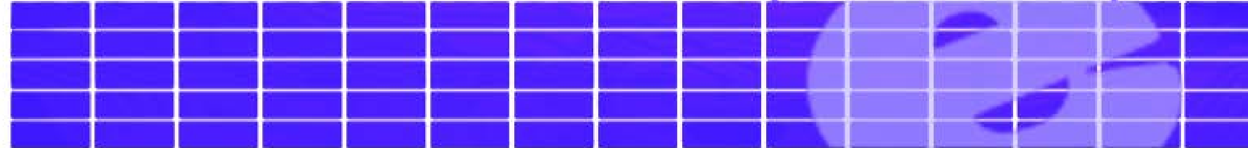


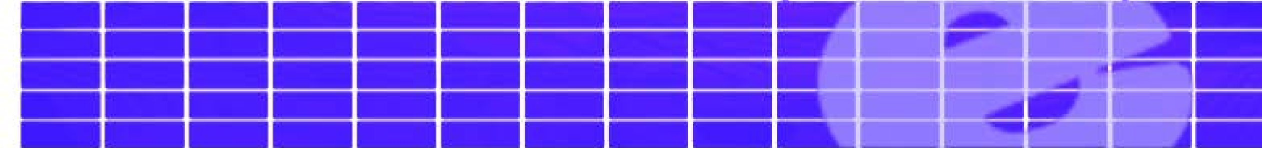
CDE'2015

10th Spanish Conference On Electron Devices

Palacio del Nuncio

Aranjuez, Spain February 11-13, 2015

www.cde2015.es



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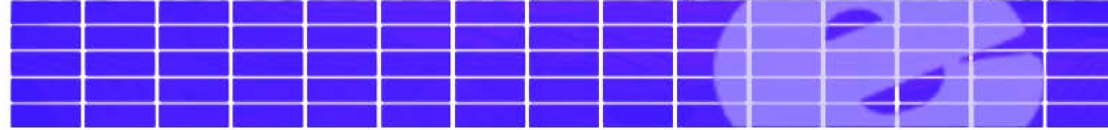


The 10th Spanish Conference on Electron Devices brings together the work of both research groups and companies on the field of electronic devices and applications. This edition will take place on February 2015, from 11th to 13th, in the so called Royal Place of Aranjuez (Madrid), carrying on with a series of previous events in Valladolid (2013), Palma de Mallorca (2011), SANTIAGO DE COMPOSTELA (2009), El Escorial (Madrid, 2007), Tarragona (2005), Calella de la Costa (Barcelona, 2003), Granada (2001), Madrid (1999) and Barcelona (1997).

Structure

The language of the Conference is English. The Conference program consists of invited and contributed papers organized in six topic sessions. This occasion THERE WILL BE three plenary talks. Contributed papers accepted for the Conference will be presented either orally or by poster. Abstract submission has to be done in pdf format through the conference webpage (paper submission tab). General guidelines for manuscript preparation can be read at the corresponding drop-down menu. Extended versions of the accepted abstracts will be published in the official Conference Proceedings, which will be distributed to PARTICIPANTS in pen drive format at the registration desk, and later available through the IEEE Xplore® database. Therefore, papers must be written in proper English and strictly follow the proposed format. There will be prizes for the best poster presented by students.

Venue

The CDE'2015 will be held on the Royal Village of Aranjuez 1, 2 (Madrid), a small city 50 km far from Madrid, which hosts a summer residence for the Royal Family and has a good, reliable transport system. Conference venue is at Palacio del Nuncio (http://palaciodelnuncio.com/). We have confidence it will provide an optimum environment for interaction between researchers. HOTELS WITH special rates for Conference participants will be made available through the Aranjuez-Venue tab.

Novelties

One of the plenary talks will be conducted by a Spanish National CONTACT Point for the Information and Communication Technologies line within the Horizon 2020 Program. A detailed overview of the different open calls in our field and the expected Spanish rate of return will be provided. Preparatory documentation will be shared at the webpage, and access to subsequent colloquium in order to discuss future proposals is scheduled.

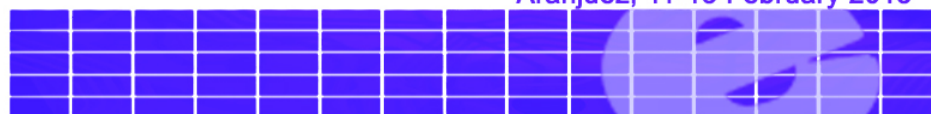
As in previous occasions a Mini-colloquium will be conducted by distinguished lecturers of the IEEE Electron Device Society Spain Section. Table of talks will be available at the Conference web.

A special oral session for students is scheduled, in which participants will briefly summarize their contributions in three minutes (either a Ph. D. Thesis, talk or poster scheduled in a subsequent session) in a similar way as done in an elevator pitch, in order to FAVOR future meetings or interaction between participants.

The necessary sobriety imposed by the current context has driven the Local Committee to hold the same registration fees approved in the previous 2013 event. Despite this sobriety, we have devoted all our resources to ensure an optimum environment for interaction.

BEST regards

CDE 2015 Local Committee



CDE 2015 HAND PROGRAM

Wednesday, Feb. 11th, 2015

10:00 h – 11:30 h REGISTRATION

14:30 h – 16:00 h SOCIAL EVENT. VISIT TO THE ROYAL PALACE OF ARANJUEZ

16:00 h – 20:00 h **SATELLITE EVENT: IEEE Electron Device Society Mini COLLOQUIUM ON ADVANCES IN NANO- AND LARGE AREA ELECTRONICS** (free attendance).

Welcome by the EDS Spain Chapter President, **Prof. Lluis Marsal**.

WELCOME TO THE STUDENTS. ELEVATOR-PITCH SESSION

Distinguished lecturers: **Tibor Grasser** (*Technische Universität Wien, Au*), **Jamal Deen** (*McMaster University, CA*), **Lluis Marsal** (*U. Rovira I Virgili, SP*), **Arokia Nathan** (*Cambridge University Centre for Advanced Photonics and Electronics*, UK), **Benjamin Iñiguez** (U. Rovira I Virgili, SP)

18:00 h – 19:30 h REGISTRATION.

20:00 h – 20:15 h WELCOME RECEPTION ON BEHALF OF MUNICIPAL, AND ACADEMIC AUTHORITIES FROM UNIVERSIDAD REY JUAN CARLOS

20:30 h – 21:00 h Universidad Rey Juan Carlos CHAMBER CHOIR PERFORMANCE.

21:00 h RECEPTION COCKTAIL (*Courtyard, Palacio del Nuncio*)

Thursday, Feb. 12th, 2015

8:00 h – 8:30 h REGISTRATION

8:30 h – 8:45 h OPENING: **Prof. Ramón Alcubilla**, *President of the Spanish CDE.*

8:45 h – 9:30 h PLENARY TALK: **D. Fernando Martín Galende**, *EU Programmes Division - Spanish ICT National Contact Point – Horizon 2020*

9:30 h – 11:35 h **SESSIONS 1 and 3:** Graphene, new materials, and device processing technology.

11:35 h – 12:00 h COFFEE BREAK

12:00 h – 13:45 h SESSION 4a: Sensors, actuators and micro/nano systems

13:45 h – 15:00 h LUNCH

15:00 h – 16:30 h SOCIAL EVENT: VISIT TO THE GARDENS OF THE ROYAL PALACE.

16:45 h – 17:25 h **IEEE EDS Mini-COLLOQIUM, FINAL SESSION. Distinguished Lecturer: Enrico Sangiorgi** *(Universita degli Studi di Bologna, IT)*. (Free entrance).

17:30 h – 18:30 h SESSION 4b: Sensors, actuators and micro/nano systems

18:30 h – 18:45 h COFFEE BREAK

18:45 h – 19:25 h SESSION 2a: Device modeling and simulation.

19:25 h – 20:45 h MAIN POSTER: SESSION (all posters are exhibited)

CDE Committee Meeting

21.00 h - GALA DINNER

Friday, Feb. 13th, 2015

8:45 h – 9:30 h PLENARY TALK (**Prof. George Malliaras**, *Head Department of Bioelectronics, ENSM- Centre Microélectronique de Provence -EMSE, MOC*)

9:30 h – 10:55 h SESSION 2b. Device modeling and simulation.

10:55 h – 11:20 h COFFEE BREAK AND CONTINUATION OF POSTER SESSION

11:20 h – 13:20 h SESSION 5a. Characterization and reliability.

13:30 h – 15:00 h LUNCH

15:00 h – 15:40 h SESSION 5b. Characterization and reliability

15:45 h – 16:30 h PLENARY TALK (**Prof. J. Bisquert**, *Departamento de Física. Universitat Jaume I de Castelló*)

16:30 h – 19:00 h SESSION 6. Optoelectronic, photovoltaic devices and displays. Hybrid and organic electronics.

17:30 h – 17:50 COFFEE BREAK.

18:50 h – 19:15 h POSTER SESSION FINAL DISCUSSIONS 2

19.15 h - 20.00 h. AWARDS CEREMONY.CLOSING REMARKS

EDS: Best Student Award

.

Wednesday, Feb. 11th, 2015

10:00 h - *Palacio del Nuncio, entrance hall*

REGISTRATION

14:30 h – 16:00 h *Aranjuez Village*
VISIT TO THE ROYAL PALACE OF ARANJUEZ.

16:00 h – 18:15 h *Auditorium, Palacio del Nuncio.*

IEEE Electron Device Society MINICOLLOQUIUM ON ADVANCES IN NANO- AND LARGE AREA ELECTRONICS (free attendance). Welcome by the EDS Spain Chapter. **Prof. Benjamin Iñiguez**. *Chair*

WELCOME TO THE STUDENTS. ELEVATOR-PITCH SESSION

SESSION A. Distinguished lecturers:

- **Prof. Arokia Nathan** (*Cambridge University Centre for Advanced Photonics and Electronics,* UK)

-- Amorphous Oxide Technology for Large Area Electronics: From Devices to Circuits and Systems, Facilitated by CAD –

- **Prof. Benjamín Íñiguez** (*U. Rovira I Virgili, SP*)

-- Compact modeling of junctionless transistors --

- **Prof. Jamal Deen** (*McMaster University, CA*)

-- Flexible Electronics – Opportunities and Challenges --

18:15 h – 18:30 h *Courtyard, Palacio del Nuncio*

EDS Mini-Colloquium COFFEE BREAK

18.30 h - 19.45 h SESSION B. Prof. **Prof. Benjamín Íñiguez,** *Chair.*

Distinguished lecturers:

- **Prof. Tibor Grasser** (*Technische Universität Wien, Au*)

- **Prof. Lluis Marsal** (*U. Rovira I Virgili, SP*)

-- Nanostructured polymer solar cells: fabrication, characterization and modeling --

20:00 h – 20:15 h *Auditorium, Palacio del Nuncio*
WELCOME RECEPTION ON BEHALF OF MUNICIPAL, AND ACADEMIC AUTHORITIES FROM UNIVERSIDAD REY JUAN CARLOS.

Universidad Rey Juan Carlos CHAMBER CHOIR performance (program at the "Final Program" web site)

21:00 h – *Courtyard, Palacio del Nuncio*
RECEPTION COCKTAIL

Thursday, Feb. 12th, 2015

8:00 h - *Palacio del Nuncio, entrance hall*

REGISTRATION

8:30 h – 8:45 h *Auditorium, Palacio del Nuncio*
OPENING: **Prof. Ramón Alcubilla**, *President of the Spanish CDE*

8.45 h - 9.30 h PLENARY TALK: **Fernando Martín Galende**, *EU Programmes Division - Spanish ICT National Contact Point – Horizon 2020*

9.30 h - 11.35 h *Auditorium, Palacio del Nuncio*
SESSIONS 1 and 3: Graphene, new materials, and device processing technology
Chairperson

9.30 h - 9.50 h

O.1.1. *In situ TEM study of reduction of graphene oxide by Joule heating*

Gemma Martín[a,*], Aïda Varea[a], J.M. Rebled[a,b] Ruben Sánchez-Hidalgo[c], David López-Díaz[c], M. Mercedes Velázquez[c], Albert Cirera[a], Francesca Peiró[a], Sònia Estradé[a] and Albert Cornet[a]
[a]MIND/IN2UB, Departament d'Electrònica, Universitat de Barcelona, Marti i Franqués 1, 08028 Barcelona, Spain
[b]CCiT, Universitat de Barcelona, C/Lluís Solé i Sabaris 1, 08028 Barcelona, Spain
[c]Dto de Química Física, Facultad de Ciencias Químicas. Universidad de Salamanca, E37008 Salamanca, Spain

9.50 h - 10.10 h

O.1.2. *Dry etching of graphene: from nanodots to microwires*

Carmen Coya[1], Miguel García-Vélez[1], Angel Luis Álvarez[1], Esteban Climent-Pascual[2], Carmen Munuera[2] and Alicia de Andrés[2]
[1] Escuela Técnica Superior de Ingeniería de Telecomunicación (ETSIT), Universidad Rey Juan Carlos, 28933 Madrid, Spain
2 Instituto de Ciencia de Materiales de Madrid, Consejo Superior de Investigaciones Científicas, Cantoblanco, Madrid, 28049, Spain

10.10 h - 10.30 h

O.1.3. *Influence of Doping on the Optical Response of GaInP*

E. Ochoa-Martínez[a],*, M. Gabás[a], L. Barrutia[b], M. Ochoa[b], I. Rey-Stolle[b], E. Barrigón[b], Carlos Algora[b]
[a]Universidad de Málaga, The Nanotech Unit, Departamento de Física Aplicada I, 29071 Málaga, Spain
[b]Instituto de Energía Solar, Universidad Politécnica de Madrid, Avda. Complutense 30, 28040 Madrid, Spain.

10.30 h - 10.50 h

O.1.4. *On the growth mechanisms of GaAs nanowires by Ga-assisted chemical beam epitaxy*

C. García Núñez, A.F. Braña, N. López and B.J. García
Grupo de Electrónica y Semiconductores. Dpto. Física Aplicada. Universidad Autónoma de Madrid..

10.50 h - 11.10 h

O.1.5. *Automatic transfer of graphene and its electrical characterization*

Alberto Boscá[1, 2*], J. Pedrós[1, 3], A. Ladrón de Guevara[1], J. Martínez[1, 4], F. Calle[1, 2, 3]
[1]Instituto de Sistemas Optoelectrónicos y Microtecnología, Universidad Politécnica de Madrid, Madrid, 28040, Spain
[2]Dpto. Ingeniería Electrónica, E.T.S.I de Telecomunicación, Universidad Politécnica de Madrid, Madrid, 28040, Spain
[3]Campus de Excelencia Internacional, Campus UCM-UPM, Madrid, 28040, Spain
[4]Dpto. de Ciencia de Materiales, E.T.S.I de Caminos, Canales y Puertos, Universidad Politécnica de Madrid, Madrid, 28040, Spain.

11.10 h - 11.30 h

O.1.6. *Chemical vapour deposition of 3D graphene foams: synthesis, properties, and applications*

J. Pedrós[1,2 *], A. Boscá[1,3], P. Bonato[1], J. Martínez[1,4], E. Climent[5], A. de Andrés[5], and F. Calle[1,2,3]
[1]Instituto de Sistemas Optoelectrónicos y Microtecnología, Universidad Politécnica de Madrid, Madrid, 28040, Spain
[3]Dpto. Ingeniería Electrónica, E.T.S.I de Telecomunicación, Universidad Politécnica de Madrid, Madrid, 28040, Spain
[2]Campus de Excelencia Internacional, Campus Moncloa UCM-UPM, Madrid, 28040, Spain
[4]Dpto. de Ciencia de Materiales, E.T.S.I de Caminos, Canales y Puertos, Universidad Politécnica de Madrid, Madrid, 28040, Spain.

11:30 h – 11:55 h *Courtyard, Palacio del Nuncio*
COFFEE BREAK

12.00 h - 13.45 h *Auditorium, Palacio del Nuncio*

SESSION 4 a : Sensors, actuators and micro/nano systems

Chairperson

12.00 h - 12.20 h

O.4.1. *Microsensors for the multiparametric analysis of natural gas quality*

Irene Castro-Hurtado[1], Isabel Ayerdi[1], Enrique Castaño[1], Angel Mª Gutierrez[2], Juan Ramón Arraibi[2]
[1]Microelectronics and Microsystems Unit, CEIT and Tecnun (University of Navarra), Paseo Manuel de Lardizabal 15, 20018-San Sebastián, Spain
[2]EDP NATURGAS ENERGIA, General Concha 20, 48010-Bilbao, Spain

12.20 h - 12.40 h

O.2.1. *DC SHEs on GaN HEMTs varying substrate material*

Raúl Rodríguez[1], Benito González[1], Javier García[1], Fetene Mulugeta[2], José María Tirado[3], Benjamín Iñiguez[2], and Antonio Núñez[1]
[1] Institute for Applied Microelectronics (IUMA), ULPGC, Las Palmas de G.C., Spain; email: rrodriguez@iuma.ulpgc.es
[2] Department of Electric, Electronic and Automation Engineering, URV, Tarragona, Spain
[3] Department of Electric, Electronic, Automation and Communications Engineering, UCLM, Toledo, Spain.

12.40 h - 13.00 h

O.4.3. *ZnO conductometric sensor for indoor air quality measurement inside buildings*

J. González-Chávarri[1,2], I. Castro-Hurtado[1,2], I. Ayerdi[1,2], E.Castaño[1,2], G.G. Mandayo[1,2]
[1]CEIT and Tecnun (Universidad de Navarra),P.Mikeletegi 48, 20009 San Sebastián, Spain
[2]CIC microGUNE, Goiru Kalea 9 Polo Innovación Garaia, 20500 Arrasate-Mondragón, Spain.

13.00 h - 13.20 h

O.4.4. *Piezoresistive cantilever force sensors based on polycrystalline silicon*

L.G. Villanueva[1], G. Rius[2], F Pérez-Murano, J Bausells
Barcelona Microelectronics Institute, IMB-CNM (CSIC), Campus UAB, E-08193 Bellaterra, Spain.
[1] EPFL, BM 5134 - Station 17, CH-1015 Lausanne, Switzerland.
[2] Nagoya Institute of Technology, NITech, Gokiso, Showa, 466-8555 Nagoya, Japan.

13.20 h - 13.40 h

O.4.5. *Liquid-crystalline pushing micropillars as actuators for haptic devices*

N. Torras[a], A. Sánchez-Ferrer[b], K.E. Zinoviev[a], J. Esteve[a]
[a] Instituto de Microelectrónica, IMB-CNM (CSIC), Campus UAB, Bellaterra, E-08193 Barcelona, Spain.
[b] ETH Zurich, Department of Health Sciences & Technology, Institute of Food, Nutrition & Health, Food & Soft Materials Science Group, Schmelzbergstrasse 9, CH-8092 Zurich, Switzerland.

13:45 h – 15:00 h *Dining room, basement, Palacio del Nuncio*
LUNCH

15:00 h – 16:30 h *Aranjuez village*
VISIT TO THE GARDENS OF THE ROYAL PALACE

16:45 h – 17:25 h Auditorium*, Palacio del Nuncio.*
IEEE Electron Device Society MINICOLLOQUIUM ON ADVANCES IN NANO- AND LARGE AREA ELECTRONICS (free attendance). **Prof. Lluis Marsal**, EDS Spain Chapter *Chair*
FINAL SESSION. Distinguished lecturer:
- **Prof. Enrico Sangiorgi** (*Universita degli Studi di Bologna, IT*)
-- Micro-nanopower systems for energy harvesting --

17.30 h - 18.30 h *Auditorium, Palacio del Nuncio*
SESSION 4 b : Sensors, actuators and micro/nano systems
Chairperson

17.30 h - 17.50 h

O.4.6. *Ge nanowire-based gas sensor fabricated by localized growth on microhotplates*

J. Samà[1], S. Barth[2], J.D. Prades[1], M. Seifner[2], O. Casals[1], I. Gracia[3], J. Santander[3], C. Calaza[3], L. Fonseca[3], C. Cané[3], A. Romano-Rodríguez[1]
[1] Universitat de Barcelona (UB), MIND-IN2UB-Departament d'Electrònica, c/Martí i Franquès, 1, 08028 Barcelona,
Spain; tel: 93 403 91 56, FAX: 93 402 11 48, e-mail: albert.romano@ub.edu
[2] Technical University Vienna, Institute of Materials Chemistry, Getreidemarkt 9/BC/02, 1060 Vienna, Austria
[3] Consejo Superior de Investigaciones Científicas (CSIC), Institut de Microelectrònica de Barcelona-Centro Nacional de Microelectrónica, Campus UAB, 08193 Bellaterra, Spain

17.50 h - 18.10 h

O.4.7. *Hybrid Integration of VCSEL and Microlens for a Particle Detection Microoptical System*

I. Bernat[1], L. Fonseca[2], M. Moreno[1],A. Romano-Rodriguez[1]
[1] Departament de Electrònica, Facultat de Física, Universitat de Barcelona. Martí i Franquès 1, 08028 Barcelona
[2] Instituto de Microelectrónica de Barcelona, CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain.

18.10 h - 18.30 h

O.4.8. *Intracellular silicon chips: A new research line at the IMB-CNM (CSIC)*

M. Duch, R. Gómez-Martínez, S. Duran, J. Esteve, J. A. Plaza
Instituto de Microelectrónica de Barcelona, CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain.

18:30 h – 18:45 h *Courtyard, Palacio del Nuncio*
COFFEE BREAK

18:45 h – 19:25 h *Auditorium, Palacio del Nuncio*
SESSION 2 a : Device modeling and simulation
Chairperson

18:45 h - 19.05 h

O.4.2. *SiNERGY, a project on energy harvesting and microstorage empowered by Silicon technologies*

Luis Fonseca, Carlos Calaza, Marc Salleras, Gonzalo Murillo, Jaume Esteve Albert Tarancón[1], Alex Morata[1], Jose D. Santos[1], Gerard Gadea[1]
IMB-CNM (CSIC) Carrer dels Til•lers, Campus UAB Bellaterra 08193
[1]Institut de Recerca en Energia de Catalunya (IREC), Jardins de les Dones de Negre 1, 08930 Sant Adrià de Besòs, Barcelona, Spain

19:05 h – 19:25 h

O.2.2. *Low Gain Avalanche Detectors for High Energy Physics Experiments*

P. Fernández-Martínez[1*], M. Baselga[1], M. Fernández García[2], D. Flores[1], V. Greco[1], S. Hidalgo[1], G. Kramberger[3], G. Pellegrini[1], D. Quirion[1], and I. Vila[2]
[1] IMB-CNM (CSIC), Campus UAB, 08193 – Bellaterra, Barcelona (Spain)
[2] IFCA (CSIC), Av. de los Castros s/n, 39005 – Santander (Spain).
[3] Institut Jožef Stefan, Jamova 39, 1000 – Ljubljana (Slovenia)

19:25 h *Board Room Palacio del Nuncio*
CDE Committee meeting

19.25 h – 20:45 h *Courtyard, Palacio del Nuncio*
MAIN POSTER SESSION (all posters are exhibited)

21:00 h *Aranjuez Village*
GALA DINNER

Friday, Feb. 13th, 2015

8:00 h - *Palacio del Nuncio, entrance hall*

REGISTRATION

8.45 h - 9.30 h PLENARY TALK: **Prof. George G. Malliaras,**
Head Department of Bioelectronics, ENSM- Centre Microélectronique de Provence -EMSE, MOC

-- Interfacing with the Brain using Organic Electronics --

9:30 h – 10:50 h *Auditorium, Palacio del Nuncio*
SESSION 2 b : Device modeling and simulation
Chairperson:

9:30 h – 9:50 h

O.2.3. *Implementation of numerical methods for nanoscaled semiconductor device simulation using OpenCL.*
E. Coronado-Barrientos, A. Garcia-Loureiro, G. Indalecio, N. Seoane[1]
Centro de Investigacion en Tecnoloxias da Informacion (CiTIUS), Universidad de Santiago de Compostela, Santiago de Compostela, Spain.
[1] Electronic Systems Design Centre, College of Engineering, Swansea University, Wales, United Kingdom

9:50 h – 10:10 h

O.2.4. *Time-dependent physics of double-tunnel junctions*
Vincent Talbo[1], Javier Mateos[1], Sylvie Retailleau[2], Philippe Dollfus[2], Tomás González[1]
[1] Departamento de Física Aplicada, Universidad de Salamanca, Plaza de la Merced S/N, E-37008 Salamanca, Spain
[2] Institut d'Electronique Fondamentale, Université Paris-Sud, CNRS UMR 8622, F-91405 Orsay, France.

10:10 h – 10:30 h

O.2.5. *Calculation of self-heating in cryogenic InP HEMTs by Monte Carlo simulations of phonon and electron transport*
J. Mateos[1], I. Iniguez-de-la-Torre[1], H. Rodilla[2], J. Schleeh[2], J. Grahn[2], T. González[1] and A. J. Minnich[3]
[1] Dpto. Física Aplicada, Universidad de Salamanca, 37008 Salamanca, Spain
[2] Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden
[3] Division of Engineering and Applied Science, California Institute of Technology, Pasadena, CA 91125

10:30 h – 10:50 h

O.2.6. *New result for Optical OFDM in Code Division Multiple Access systems using direct detection*
A. Cherifi[1], B. Bouazza[1], A. O. Dahmane[2], B. Yagoubi [3]
[1] Laboratory Technology of Communication, University Of Tahar Moulay Saida, 138 nasr, Algeria.
[2] University of Québec à Trois-Rivières C .P. 500, Trois-Rivières, Québec, Canada / G9A 5H7
[3] University of Abdelhamid Ibn Bdis Mostaganem, Algeria.

10.55 h - 11.20 h *Courtyard, Palacio del Nuncio*
COFFEE BREAK and POSTER SESSION CONTINUATION

11.20 h - 13.20 h *Auditorium, Palacio del Nuncio*
SESSIONS 5a: Characterization and reliability

11.20 h - 11.40 h

O.5.1. *Investigation of the Resistive Switching Behavior in Ni/HfO$_2$-based RRAM Devices*
M.B. Gonzalez, M.C. Acero, O. Beldarrain, M. Zabala, and F. Campabadal

Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain

11:40 h – 12:00 h

O.5.2. *Electrical characterization of MIS capacitors based on Dy_2O_3-doped ZrO_2 dielectrics*

H. García[1], H. Castán[1], S. Dueñas[1], E. Pérez[1], L. Bailón[1], A. Tamm[2], K. Mizohata[3], K. Kukli[2], J.Aarik[2]

[1] Dept. de Electricidad y Electrónica, Universidad de Valladolid, ETSI Telecomunicación, Paseo de Belén 15, 47011 Valladolid, Spain

[2] University of Tartu, Institute of Physics, Department of Materials Science, EE-50411 Tartu, Estonia

[3] Department of Physics, University of Helsinki, P.O. Box 43, FI-00014, University of Helsinki, Finland

12.00 h - 12.20 h

O.5.3. *Amorphous/crystalline silicon interface characterization by capacitance and conductance measurements*

R. García-Hernansanz [*1,2], E. García-Hemme [1,2], D. Montero-Alvarez [1,2], J. Olea [3,2], D. Pastor [1,2], A. del Prado[1], I.Mártil[1] and G. González-Díaz[1]

[1] Dpto. Física Aplicada III,Univ. Complutense de Madrid

[2] CEI Campus Moncloa, UCM-UPM, Madrid, Spain

[3] Instituto de Energía Solar, E.T.S.I. Telecomunicación, Univ. Politécnica de Madrid.

12.20 h - 12.40 h

O.5.4. *Valence EELS analysis of multiple InGaN-QW structure for electronic properties*

A. Eljarrat[1,*], L. López-Conesa[1], C. Magén[2,3] , N. García-Lepetit[4], Ž. Gačević[4], E. Calleja[4], S. Estradé[1,5] and Francesca Peiró[1]

[1] LENS-MIND-IN2UB, Departament d'Electrònica, Universitat de Barcelona, c/ Martí i Franqués 1, 08028 Barcelona, Spain.

[2] LMA-INA, Departamento de Física de la Materia Condensada, Universidad de Zaragoza, 50018 Zaragoza, Spain

[3] Fundación ARAID, 50018 Zaragoza, Spain.

[4] TEM-MAT, Centres Científics i Tecnològics (CciT), Universitat de Barcelona, Solís Sabarís 1, Barcelona, Spain.

[5] ISOM, Universidad Politécnica de Madrid, Ciudad Universitaria s/n, 28040 Madrid, Spain.

12.40 h - 13.00 h

O.5.5. *Anomalous Low-Frequency Noise Increase at the Onset of Oscillations in Gunn Diodes*

Ó. García-Pérez[1], Y. Alimi[2], A. Song[2], I. Íñiguez-de-la-Torre[1], S. Pérez[1], J. Mateos[1], T. González[1]

[1] Dpto. Física Aplicada, Universidad de Salamanca, 37008 Salamanca, Spain

[2] School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, United Kingdom.

13.00 h - 13.20 h

O.5.6. *Impact of NBTI and CHC stress on the nanoscale electrical properties of strained and non-strained MOSFETs*

Q.Wu, M. Porti, A. Bayerl, J. Martin-Martínez, R. Rodriguez, M. Nafria, X. Aymerich, E. Simoen[1]

Dept. Enginyeria Electrònica, Universitat Autònoma de Barcelona (UAB), Barcelona, Spain

[1] IMEC, Leuven, Belgium

13:30 h – 15:00 h *Dining room, basement, Palacio del Nuncio*

LUNCH

15:00 h – 15:40 h *Auditorium, Palacio del Nuncio*

SESSION 5 b : Characterization and reliability

Chairperson

15.00 h - 15.20 h

O.5.7. *Impact of millisecond anneal induced for ultra-shallow junctions on Negative Bias Temperature Instability*

M. Moras[a], J. Martin-Martinez[a], V. Velayudhan[a], R. Rodriguez[a], M. Nafria[a], X. Aymerich[a] and E. Simoen[b]

[a] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona (UAB), Bellaterra, Barcelona, Spain

[b] IMEC, Leuven, Belgium

15.20 h - 15.40 h

O.5.8. *Thermal stability study of AlGaN/GaN MOS-HEMTs using Gd_2O_3 as gate dielectric fabricated on Si*

Z. Gao[1*], M. F. Romero[1], M. A. Pampillon[2], E. San Andres[2], F. Calle[1]

[1] Dep. Ingeniería Electrónica and Instituto de Sistemas Optoelectrónicos y Microtecnología, ETSI Telecomunicación, Universidad Politécnica de Madrid, Av. Complutense 30, 28040 Madrid, Spain

[2] Dep. Física Aplicada III (Electr. y Electron.), Univ. Complutense de Madrid, Madrid, Spain.

15.45 h - 16.25 h **PLENARY TALK: Prof. Joan Bisquert**,
Departamento de Física. Universitat Jaume I de Castelló
-- Dynamic processes in perovskite solar cells --

16:30 h – 19:00 h *Auditorium, Palacio del Nuncio*
SESSION 6 Optoelectronic, photovoltaic devices and displays. Hybrid and organic electronics.
Chairperson:

16.30 h - 16.50 h
O.6.1. *New Generation Architectures in III-V Multijunction Solar Cells for Efficiencies of 50%*
C. Algora, I. Rey-Stolle, E. Barrigón, I. García, M. Vázquez, N. Núñez, R. Peña. P. Espinet, M. Ochoa, L. Ayllón, L. Barrutia, V. Orlando, H. Pengyun, M. Gabás[1] and S. Palanco[1], C. Ballesteros[2] and B. Galiana[2]
Instituto de Energía Solar, Universidad Politécnica de Madrid
[1] Dpto. Física Aplica I, The Nanotech Unit, Universidad de Málaga
[2] Universidad Carlos III de Madrid

16.50 h - 17.10 h
O.6.2. *Spectral Coupling of Atmosphere and the Performance of Perovskite Solar Cells*
Eduardo F. Fernandez[1,2,3*], S. Senthilarasu[1], F. Almonacid[3], A. J. Garcia-Loureiro[2], T. K. Mallick[1]
[1] Environment and Sustainability Institute (ESI), University of Exeter, Penryn, Cornwall TR10 9FE, United Kingdom
[2] Centro de Investigación en Tecnoloxías da Información (CITIUS), University of Santiago de Compostela, Santiago de Compostela E15782, Spain
[3] Centro de Estudios Avanzados en Energía y Medio Ambiente (CEAEMA), University of Jaen, Jaen 23071, Spain

17.10 h - 17.30 h
O.6.3. *Deep level defects in mono-like, quasi-mono and multicrystalline silicon solar wafers*
E. Pérez, H. García, H. Castán, S. Dueñas, and L. Bailón
Dept. de Electricidad y Electrónica, Universidad de Valladolid, E.T.S.I. de Telecomunicación, Paseo de Belén 15, 47011 Valladolid, Spain.

17.30 h - 17.50 h *Courtyard, Palacio del Nuncio*
COFFEE BREAK and **POSTER SESSION CONTINUATION**

17.50 h - 18.10 h
O.6.4. *Optimizing diffusion, morphology and minority carrier lifetime in Silicon for GaAsP/Si dual-junction solar cells*
Elisa García-Tabarés[1], Diego Martín[2], Ignacio Rey-Stolle[1]
[1] Instituto de Energía Solar – Universidad Politécnica de Madrid. Avda. Complutense 30 – 28040 Madrid (Spain)
[2] Departamento de Matemática Aplicada, Ciencia e Ingeniería de los Materiales y Tecnología Electrónica. Universidad Rey Juan Carlos. CL Tulipán s/n, 28933 Móstoles, Madrid (Spain)

18.10 h - 18.30 h
O.6.5. *Degree of ordering as a function of Sb content in $In_{0.5}Ga_{0.5}P$ layers for tandem solar cells*
Ll. López[1], C. Coll[1], E. Barrigón[2], L. Barrutia[2], I. Rey-Stolle[2], S. Estradé[1], F. Peiró[1]
[1] Laboratory of Electron Nanoscopies (LENS)-MIND/IN2UB, Dept. d'Electrònica, Universitat de Barcelona, c/ Martí Franqués 1, E-08028 Barcelona
[2] Instituto de Energía Solar (IES), Universidad Politécnica de Madrid.

18.30 h - 18.50 h
O.6.6. *All-inkjet printed organic transistors: Strategies to minimize variability*
M.C. R. Medeiros [1], V. Parkula [2], C. Martinez-Domingo [3,4], E. Ramon[4], F. Villani [5], F. Loffredo[5], R. Miscioscia[5], E. Sowade[6], K. Y. Mitra[6], R. R. Baumann[6,7], I. McCulloch[8], J. Carrabina[9] and Henrique L. Gomes [2]
[1] Instituto de Telecommunicações, DEEC, FCTUC, University of Coimbra, Pinhal de Marrocos, Coimbra, Portugal.
[2] Universidade do Algarve, Instituto de Telecomunicações, Av. Rovisco, Pais, 1, Lisboa, Portugal
[3] Catalan Institute of Nanoscience and Nanotechnology (ICN2),Campus UAB Bellaterra, Barcelona, 08193 Spain.
[4] Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), Campus UAB Bellaterra, Barcelona, Catalonia, Spain.
[5] Italian National Agency for New Technologies, Energy and Sustainable Economic Development (ENEA), Portici
Research Center, 80055 Portici,Naples, Italy
[6] Chemnitz University of Technology, Digital Printing and Imaging Technology, Chemnitz, Germany.
[7] Fraunhofer Institute for Electronic Nano Systems (ENAS), Printed Functionalities, Chemnitz, Germany
[8] Department of Chemistry Imperial College London London SW7 2AZ, UK
[9] CAIAC, Universitat Autònoma de Barcelona, Bellaterra, Catalonia, Spain

18.50 h - 19.15 h *Courtyard, Palacio del Nuncio*
POSTER SESSION FINAL DISCUSSIONS

19.15 h - *Auditorium, Palacio del Nuncio*
CONCLUDING REMARKS
and **EDS BEST STUDENT CONTRIBUTION AWARD**

Contributions for POSTER SESSIONS

P.1.1- *Effect of the blistering of ALD Al2O3 films on the silicon surface in Al-Al2O3-Si structures*

M.C. Acero, O. Beldarrain, M. Duch, M. Zabala, M. B. González, and F. Campabadal. .#0016

P.1.2- *Monte Carlo Modeling of Mobility and Microscopic Charge Transport in Supported Graphene.*

Raúl Rengel, José M. Iglesias, Elena Pascual and María J. Martín. #0020

P.1.3- *On the ageing mechanisms of graphene electrodes.* #0030

Yuanyuan Shi, Yanfeng Ji, Fei Hui, Mario Lanza.

P.1.4- *Graphene devices fabricated by laser.* #0040

A. Ladrón de Guevara, A. Bosca, J. Pedros, F. Calle, J. Martinez

P.1.5- *Electrostatics and drift-diffusion current model of bilayer graphene field-effect transistors.*

Pasadas Cantos, Francisco; Jiménez Jiménez, David. #0061

P.1.6- *Simulation of the phonon-limited electron mobility in multi-layer MoS2 field-effect transistors.*

J.M. González-Medina, F. G. Ruiz, A. Godoy, E. G. Marin, F. Gámiz. #0070

P.1.7- *Graphene transferred on atomic force microscope tips provides superior performance.*

Fei Hui; Marc Porti; Montserrat Nafria; Mario Lanza. #0017

P.2.1- *3D TCAD Modeling of Laser Processed c-Si Solar Cells.* #0002

Juan M. López-González, Isidro Martín, Pablo Ortega, Albert Orpella and Ramón Alcubilla.

P.2.2- *Intrinsic factors determining the metal-graphene contact resistance.* #0009

Chaves Romero, Ferney Alveiro; Jimenez Jimenez, David.

P.2.4- *Modeling of the I-V and I-t Characteristics of Multiferroic BiFeO3 Layers.* #0010

E. Miranda, D. Jiménez, A. Tsurumaki-Fukuchi, J. Blasco, H. Yamada, J. Suñé, and A. Sawa.

P.2.5- *Floating-Body-Correlated Subthreshold Behavior of SOI NMOS Device Considering Back-Gate-Bias Effect.* #0019

S. K. Hu and J. B. Kuo.

P.2.6- *Optoelectronic properties of small defect clusters in Si from multiscale simulations.*

I. Santos, M. Aboy, P. López, L. A. Marqués, M. Ruiz, L. Pelaz #0042

P.2.7- *Modeling of nanocalorimetry experiments to investigate the kinetics of damage annealing in self-implanted Si.* #0044

Ruiz Prieto, Manuel; Pelaz Montes, Lourdes; Marqués Cuesta, Luis Alberto; López Martín, Pedro; Santos Tejido, Iván; Aboy Cebrián, María.

P.2.8- *MD simulations of vacancy-like defects in amorphous Ge.* #0045

Lopez Martin, Pedro; Sanchez Hurtado, Jose Miguel; Pelaz Montes, Maria Lourdes; Marques Cuesta, Luis Alberto; Santos Tejido, Ivan; Aboy Cebrian, Maria; Ruiz Prieto, Manuel.

P.2.9- *A charge-dependent mobility memristor model* . #0049

Picos , Rodrigo; Al-Chawa , M. Moner; Garcia-Moreno , Eugeni

P.2.10- *Geometrical effects on the quality factor of extensional microplate resonators in liquid* .

Ruiz-Díez , Víctor; Manzaneque , Tomás; Hernando-García , Jorge; Abdallah , Ababneh; Seidel, Helmut; Sánchez-Rojas , José Luis. #0064

P.2.11- *Short Channel Effects in Graphene Field-Effect Transistors.* #0066

Feijoo Guerro, Pedro Carlos; Jiménez Jiménez, David

P.2.12- *Impact of the Absorption in Transmittance and Reflectance on Macroporous Silicon Photonic Crystals.* #0072

Cardador Maza, David; Vega Bru, Didac; Rodriguez Martinez, Angel .

P.2.13- *Raytracing and electromagnetic 2-D simulations of the EQE of a-Si:H thin-film solar cells.*

M. Fortes, E. Comesaña, J.A. Rodriguez, P. Otero, A. J. Garcia-Loureiro #0021

P.2.14- *A tool to deploy nanodevide simulations on Cloud.* #0038

F. Gomez-Folgar, G. Indalecio. E. Comesaña, A. J. Garcia-Loureiro, T. F. Pena

P.2.15- *Evaluation of the Thermal Resistance in GaN-Diodes by means of Electro-Thermal Monte Carlo Simulations.* #0043

S. García, I. Íñiguez-de-la-Torre, Ó. García-Pérez, J. Mateos, T. González and S. Pérez

P.2.16- *Comparison of state-of-the-art distributed computing frameworks with the GWM.* #0074

G. Indalecio, F. Gómez-Folgar, A. J. Garcia-Loureiro, Natalia Seoane

P.2.17- *Influence of systematic gate alignment variations on static characteristics in DG-SB-MOSFETs.*

José M. Iglesias*, María J. Martín, Elena Pascual, Raúl Rengel #0092

P.4.1- *Flexible gas sensing devices with directly grown tungsten oxide nanoneedles via AACVD.*

Vallejos Vargas, Stella; Gràcia Tortadés, Isabel; Figueras Costa, Eduardo; Sánchez López, Javier; Mas Colomina, Roser; Beldarrain Fernández, Oihane; Cané Ballart, Carles #0005

P.4.2- *RADFET response to photon and electron beams.* #0011

Martínez Garcia, María Sofía; Torres del Rio, Julia; Banqueri Ozáez, Jesús; Carvajal Rodríguez, Miguel Angel; Palma López, Alberto José.

P.4.3- *Comparative study of printed capacitive sensors.* #0013

Rivadeneyra Torres, Almudena; Fernández Salmerón, José; Agudo Acemel, Manuel; Capitán Vallvey, Luis Fermín; Palma López, Alberto; López Villanueva, Juan Antonio.

P.4.4- *Synthesis and characterization of SnO2 nanowires grown by CVD for application as gas sensors* .

Sayago , Isabel ; Fernández , María Jesús; Fontecha , José Luis; Horrillo, Mari Carmen; Santos , José Pedro. #0018

P.4.5- *Liquid characterization by means of Love-wave device combined with microfluidic platform.* #0027

D. Matatagui, M.J. Fernandez, J. Fontecha, J.P. Santos, I. Sayago, I. Gràcia, C. Cané, M.C. Horrillo.

P.4.6- *Use of an electronic nose as a tool to differentiate winemaking techniques.* #0041

M. Aleixandre, J.P. Santos, I. Sayago, J.M. Cabellos, T. Arroyo, M.C. Horrillo.

P.4.7- *Real time detection of beer defects with a hand held electronic nose.* #0053

Santos Blanco, José Pedro; Lozano Rogado, Jesús.

P.4.8- *Compact Device for CO2 Optical Sensing using Macroporous Silicon Photonic Crystals.*

Vega Bru, Didac ; Trifonov , Trifon; Calavia Boldu, Raül; Vilanova Salas, Xavier; Rodríguez Martínez, Ángel. #0069

P.4.9- *Microfluidic platform with absorbance sensor for glucose detection.* #0055

G. Flores, F. Perdigones, C. Aracil, M. Cabello and J.M. Quero.

P.4.10- *A New Kind of Miniature Sun Sensors Design.* #0091

Wang Sui'an, Li Peihao, Guo Qi

P.4.11- *Design of an enhanced MEIGA-MetNet dust micro-sensor able to perform gas sensing in Mars atmosphere.* #0093

Miguel A. Rodríguez, Alberto Fernández, Francisco Cortés, Fernando López

P.5.1- *Single Event Transients Generation in Silicon Devices with Pulsed Laser. A comparative Study.*

De Paul , Ivan; Bandi , Franco; Segura, Jaume; Bota, Sebastià A. . #0003

P.5.2- *Performance of Advanced Metering Infrastructure Using Cellular Communication based on Uplink CDMA.* #0029

Rodriguez Morocho, Guillermo.

P.5.3- *Low dose radiation effects on a-Si:H TFTs.* #0032

Picos , Rodrigo; Papadopoulos , Nikolaos P.; Lee , Czang-Ho; Lopez-Grifols , Alvaro; Roca , Miquel; Isern , Eugeni; Wong , William S.; Garcia-Moreno, Eugeni.

P.5.4- *Straightforward Determination of the Effective Mobility-Lifetime Product of Small Molecule Organic Solar Cells.* #0048

Gerling Sarabia, Luis Guillermo; Amahdpour, Mehrad; Galindo Lorente, Sergi; Asensi López, José Miguel; Voz Sánchez, Cristobal; Puigdollers González, Joaquim; Alcubilla González, Ramón.

P.5.5- *Radiation Effects in nanometric SRAMs induced by 18 MeV Protons.* #0062

Daniel Malagón Periánez, J.L. Merino, G. Torrens, J. Segura, S.A. Bota

P.5.6- *Distinguishing conductive filament and non-localized gate conduction in resistive switching devices.* #0007

M. Maestro, A. Crespo-Yepes, J. Martin-Martinez, S. Claramunt, R. Rodriguez, M. Nafria, X. Aymerich

P.5.7- *The Meyer-Neldel Rule in the properties of the deep-level defects present in silicon supersaturated with titanium.* #0025

E. Pérez, H. Castán, H. García, S. Dueñas, L. Bailón, D. Montero, R. García-Hernansanz, E. García-Hemme, J. Olea, and G. González-Díaz.

P.5.8- *Optoelectronic properties of embedded silicon nanocrystals by hyperspectral low-loss EELS.*

A. Eljarrat, L. López-Conesa, J. López-Vidrier, S. Hernández, S. Estradé, C. Magén, B. Garrido and F. Peiró. #0046

P.5.9- *XPS and SEM as diagnosis tools for failure analysis after reliability tests performed on III-V multijunction solar cells.* #0076

V. Orlando, M. Gabás, P. Espinet-González, R. Romero, M. Vázquez, S. Bijani, N. Núñez, S. Palanco, C. Algora.

P.6.1- *High efficiency interdigitated-back-contact c-Si solar cells.* #0004

E. Calle, P. Ortega, G. López, I. Martín, D. Carrió, C.Voz, A. Orpella, J. Puigdollers, R. Alcubilla.

P.6.2- *Effect of doping in the current voltage characteristics of organic diodes* . #0012

P. López Varo, J. A. Jiménez Tejada, J. A. López Villanueva, M. J. Deen.

P.6.3- *Effect of nanofluid conductivity and humidity on the self-assembly of colloidal crystals by means of electrospray.* #0022

Arnau Coll, Sandra Bermejo, Isidro Martin and Luis Castañer.

P.6.4- *Feasibility of dispensing technology to create local contacts on silicon solar cells.*

Elena Navarrete Astorga, Miguel Marín Enríquez, José Ramón Ramos Barrado . #0035

P.6.5- *Synthesis of PbS/Semiconducting Polymer Nanocomposites Via Thiolate Decomposition.*

J.C. Ferrer, S. Fernández de Ávila, J.L. Alonso. #0060

Abstracts

Microsensors for the multiparametric analysis of natural gas quality

Irene Castro-Hurtado[1], Isabel Ayerdi[1], Enrique Castaño[1], Angel Mª Gutierrez[2], Juan Ramón Arraibi[2]

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[2]EDP NATURGAS ENERGIA, General Concha 20, 48010-Bilbao, Spain

1. Abstract

Natural gas composition varies depending on its point of origin and on its manipulation during the distribution to end users. This change of composition, which must be accurately measured, affects the chemical and physical properties of the natural gas. There are two key parameters that depend on the composition of natural gas and that affect energy billing and industrial processes. First, the High Calorific Value (HCV), which is an indicator of the heat quantity supplied. Secondly, the Methane Number (MN), a parameter used to prevent knocking in gas engines. The aim of this work is to implement a series of novel multiparametric techniques based on micro-nanotechnology to evaluate the quality of natural gas. The advantage of the method proposed is that the HCV or NM of the gas mixture are measured by indirect methods employing MEMS, this means that low cost and combustion-less process is carried out..

2. Experimental

Two different sensors, figure 1, were developed by means of microfabrication techniques. The major advantage of the fabrication process is that it is suitable for mass production and provides low cost sensors. HCV sensor consists on a surface acoustic wave sensor (SAW). This sensor was fabricated on ST-cut quartz substrate, which is a piezoelectric material. The transmitting and receiving interdigital transducers (IDTs) were obtained by sputtering of aluminum followed by patterning with photolithographic technique. A thermal conductivity sensor is employed to determine the MN. This sensor was fabricated on silicon substrate, where Si_3N_4 thin film was deposited by LPCVD. In the next step, Pt resistance was deposited and an annealing treatment in Ar was carried out to stabilize the microstructure of the Pt film. Finally, silicon etching was carried out in TMAH solution to remove the silicon beneath the resistance and obtain a micro-bridge. The microsensors were tested under 5 different mixtures of natural gas, obtained by varying the molar percentage of each component of the mixture (methane, ethane, propane, butane, CO_2 and N_2).

3. Results and discussion

A Surface Acoustic Wave (SAW) sensor is employed to measure the variation of viscosity of the natural gas. The viscosity and density of the surrounding medium affects the propagation of the wave, so a relation between the amplitude and frequency of the sensor and dynamic viscosity can be obtained. Figure 2 shows the response of a sensor (10 μm width) under different samples with different dynamic viscosity. As shown in Figure 3, the amplitude of insertion losses (ΔIL/IL0) decreases when the gas mixture presents a bigger $\eta*\rho$. This means that a higher density and viscosity of the gas gives rise to the signal attenuation. In this way, if the higher molecular weight hydrocarbons are present in a greater percentage in the gas mixture, the sensor signal will be decreased. On the other hand, a thermal conductivity sensor is employed to determine the methane number of the gas mixture. Figure 4 shows the voltage evolution of the sensing resistance when the sample is tested under different natural gas mixtures. The samples characterized with a higher thermal conductivity dissipate more heat and a decrease in the output signal and the temperature achieved by the resistance is produced. For the range of thermal conductivities considered (0.0307-0.0354 W/mK), the microsensor gives an output signal of 48 mV and a good linearity. Furthermore, the thermal conductivity of the gas mixture can be related to the MN, so a linear relationship is described for the MN and output voltage.

4. Conclusions

In this work two fundamental parameters of natural gas have been determined by means of indirect measurements. For this purpose, two physical properties of the mixture have been controlled: the dynamic viscosity of the gas and the thermal conductivity. Two low cost sensors have been fabricated by thin film technology and tested under different natural gas compositions. These microsensors provide an accurate relationship between the parameter to be determined and the physical property measured.

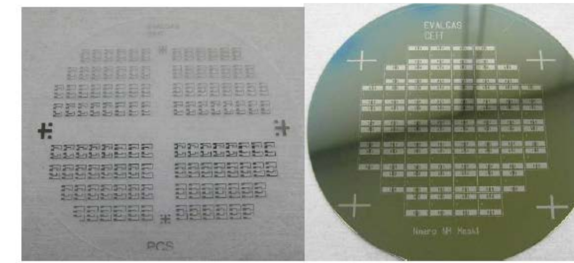

Fig.1. *ST-cut Quartz Wafer provided with HCV sensors (left) and silicon wafer with NM sensors (right).*

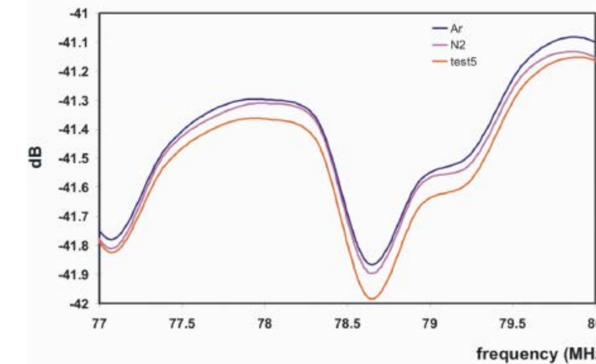

Fig 2. *Response to different gas mixtures of a SAW sensor with f0=78.9 MHz.*

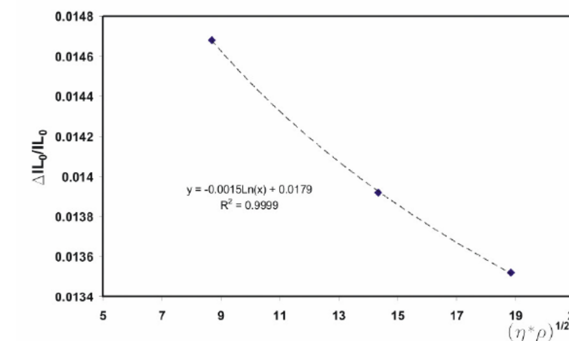

Fig 3 *Amplitude of insertion losses of the SAW sensor under different test gas mixtures.*

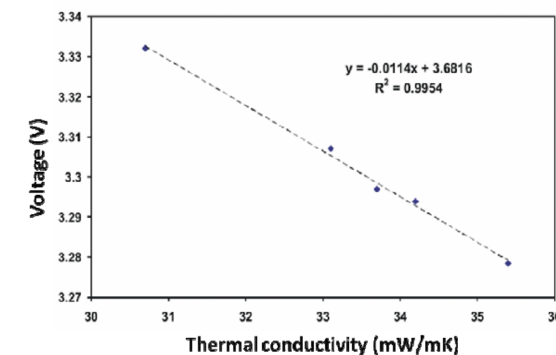

Fig 4. *Voltage variation as a function of thermal conductivity of the gas for different natural gas mixtures.*

3D TCAD Modeling of Laser Processed c-Si Solar Cells

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1. Introduction

Laser-fired contact (LFC) is a cost effective technique successfully applied to form the rear contact of Passivated Emitter and Rear Cell (PERC) high efficiency crystalline silicon (c-Si) solar cells [1]. Modeling of LFC-PERC c-Si solar cells requires 3D TCAD tools because approximating a point-like contact with one or two-dimensional geometries leads to significant errors in the calculation of resistive and recombination losses [2]. In this study, we show 3D TCAD optical and electrical models and parameters for the simulation of LFC-PERC silicon solar cells. The model is verified through experimental measurements on FZ Silicon p-type substrates. Finally, the model is extended to simulate the results of a new c-Si solar cell fabrication technology called DopLa (Doped by Laser) cell, where all the highly doped regions of the device are based on laser processed dielectric films.

2. Device Modeling

Fig.1 and Table 1 show 3D basic domain for solar cell geometry and parameters used in the simulation of LFC-PERC on 2.2 Ωcm FZ p-type substrate. Details of the fabrication process are shown in [3]. The physical model using 3D-ATLAS software [4], takes into account: Fermi-Dirac statistics, bandgap narrowing with appropriate Silicon intrinsic concentration, band-to-band recombination, Kerr-Cuevas Auger recombination model, and surface recombination parameters. Reflectance losses are modeled through the modification of the AM1.5G solar spectrum. The ohmic losses related to the front metallization are introduced by means of a front distributed contact resistance. A rear contact resistance is included at the back electrode.

3. Results

We used the previously described model to reproduce the photovoltaic features of LFC back contacted solar cells with distance between rear contact or *pitch* ranging from 200 to 800 µm. Fig. 2 shows the experimental and simulated values for short-circuit current density (J_{sc}), open circuit voltage (V_{oc}), fill factor (FF), and energy conversion efficiency (η). Our model fits experimental values using a minority carrier recombination velocity at the rear contacts of 3.5 x 10^4 cm/s and a rear contact resistance of 2 mΩcm^2. This simulation model can be used to study new crystalline silicon (c-Si) solar cells. Our lab is developing a new c-Si solar cell technology based on the laser processing of dielectric films in order to create all the highly-doped regions called DopLa (Doped by Laser) cell [5]. Fig. 3 shows the DopLa cell structure. The front face has the same configuration as the rear surface of the LFC-PERC simulated cells. Thus, the verified model can be directly applied to it. On the other hand, the rear surface consists of a hexagonal matrix of n$^+$ laser doped regions with pitches from 200 to 350 µm. Fig. 4 presents J-V curves under dark and illumination conditions for both simulated and experimental results. As it can be seen, the model is able to reproduce the experimental data allowing a deeper understanding of this device. Particularly, the rear surface is modeled by a positive fixed charge density (Q_f) of 4.3 x 10^{11} cm^{-2}, which includes the effect of different work functions between rear metal and c-Si substrate, and a fundamental surface recombination velocity ($S_{,rear}$) of 3000 cm/s equal same for electrons and holes. These results suggest the creation of an inversion layer emitter on this surface that helps in the photogenerated carrier collection.

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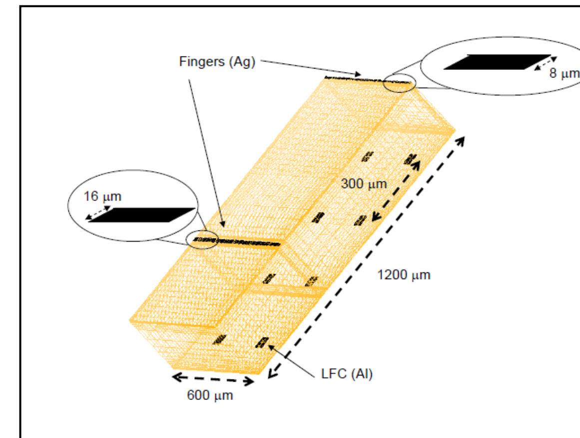

Fig.1. Basic domain for solar cell of pitch 300.

Carrier statistics	Fermi-Dirac
Energy gap	1.12 eV at 300 K
Bandgap narrowing	Slotboom model, $n_{i,eff}$=8.56 x 19^{9}cm^{-3} at 298 K
Carrier mobility	Caughey-Thomas model
Sockley-Read-Hall	Defect level at midgap $\tau_{n0}=\tau_{p0}$=0.5 s
Auger	Kerr-Cuevas model $C_{An,l}$ = 2.2 x 10^{-31} cm^6/s, $C_{Ap,l}$ = 9.9 x 10^{-32} cm^6/s, and $C_{A,h}$ = 1.66 x 10^{-30} cm^6/s
Radiative	C_{BB}=4.7 x 10^{-15} cm^3/s
Rear contacted surface	Surface recombination model: $J_n=qS_n(n-n_0)$ and $J_p=qS_p(p-p_0)$
Rear passivated surfaces	Defect level at mid-gap and S_{nO} and S_{p0} model and Q_f fixed charge density model
Front passivated surfaces	Defect level at mid-gap and S_{nO} and S_{p0} model
n$^+$ emitter region	Gaussian distribution, surface concentration 10^{19} cm^{-3} and junction depth 1 µm
Acceptor density, N_A	6.5 x 10^{15} cm^{-3} leading to ρ = 2.2 Ωcm (for 2.2 Ωcm FZ p-type substrate) and 3.6 x 10^{16} cm^{-3} leading to ρ = 0.45 Ωcm (for DopLaCell)

Table 1. Summary of the most relevant parameters used in the 3D TCAD simulation.

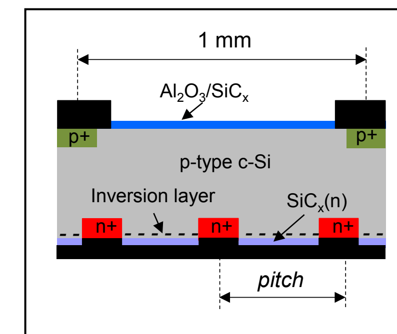

Fig.3. Sketch of DopLa (Doped by Laser) cell structure.

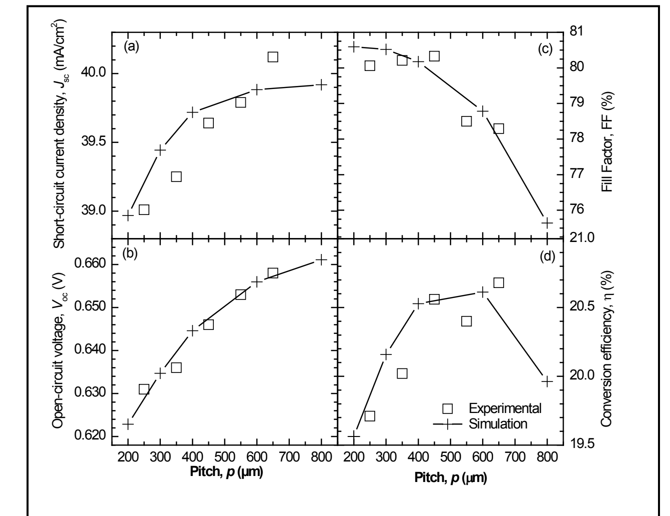

Fig.2. Experimental and simulated 3D-TCAD photovoltaic parameters for c-Si 2.2 Ωcm FZ p-type substrate solar cells with pitch from 200 to 800 µm.

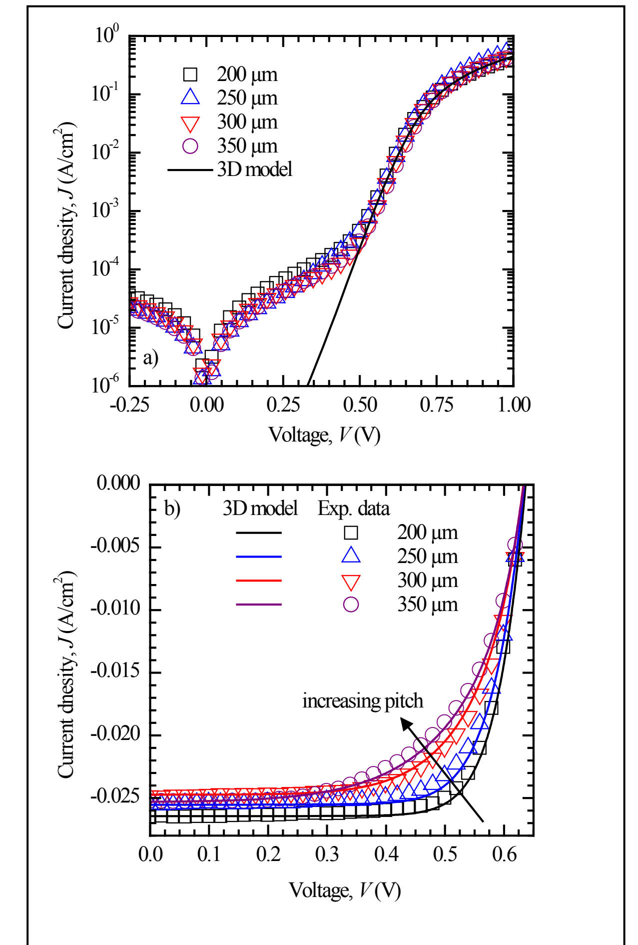

Fig.4. Experimental and simulated (3D) J-V dark and illuminated characteristics of DopLa (Doped by Laser) solar cells with pitch from 200 to 350 µm.

Single Event Transients Generation in Silicon Devices with Pulsed Laser. A comparative Study

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1. Abstract

In this work we performed a comparative study of the characteristics and capabilities of a pulsed laser system for single event injection available at the UIB referred to similar pulsed laser test facilities available in Europe (EADS, IMS) and the United States (JPL, NRL). A series of experimental measurements were carried out on a silicon photodiode (Centronics OSD15-5T) that was used in a previous comparative study conducted by the mentioned centers. In addition, this study allows us to perform a reliability characterization concerning SEEs (single event effects) and soft errors.

2. Objectives

The goal of this study is analyze the response of a photodiode against ultra-short pulse laser (lower than 1ps), that emulates the hit of high energy particles, in order to understand how charge carrier generation mechanism works inside the PN junction and how reverse bias and light intensity affects transient amplitude and collected charge.

3. Experimental Results

Fig. 1 shows the fotocurrent transient generated at the fotodiode. The transients can be approximated by a double exponential function [1]:

$$I(t)=\frac{Q}{\tau_1-\tau_2}\left(e^{-t/\tau_1}-e^{-t/\tau_2}\right)$$

Where Q is the total collected charge and τ_1 and τ_2 are two time constants controlling the rise-time of the leading edge and the decay. This fitting accepts a wide range of reverse bias polarization and focusing distances. However, if the beam is focused at the surface, the behaviour of the transient cannot be explained by a double exponential due to effects like Auger recombination, funneling or a collapse of the electric field at the depletion region.

Fig. 2 reveals a dependence of peak amplitude with focusing. With high carrier densities there is an increase of time constants of double exponential fitting. This behaviour may be attributed to a collapse of the electric field in the depletion region due to the high carrier density injected by the beam [2].

Fig. 3 shows the collected charge as a function of defocusing distance. Collected charge was calculated integrating the photocurrent. At surface focus the collected charge has a minimum, this decrease of the ratio between collected charge and pulse energy can be explained by an increase of electron-hole pair recombination [2].

As a way of compare collected charge results, pulse energy of our laser was normalized to a pulse of λ = 1064 nm. Fig. 4 represents the collected charge as a function of corrected energy. The results measured at the UIB set-up follow the same trend that the the results reported at [2].

4. Conclusions

This work shows how the response of a PN junction varies as a function of reverse bias polarization and light intensity (focus distance). The experimental transients can be fitted by a double exponential function. We also found that the performance of our laser system match with those of other European and American pulsed-laser facilities with similar characteristics.

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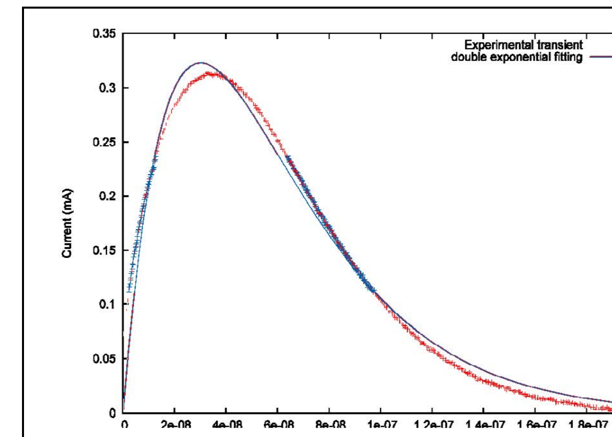

Fig.1. (red) Current transient produced by the laser pulse (focused pulse at V_D=-12 V). (blue) Double exponential fitting.

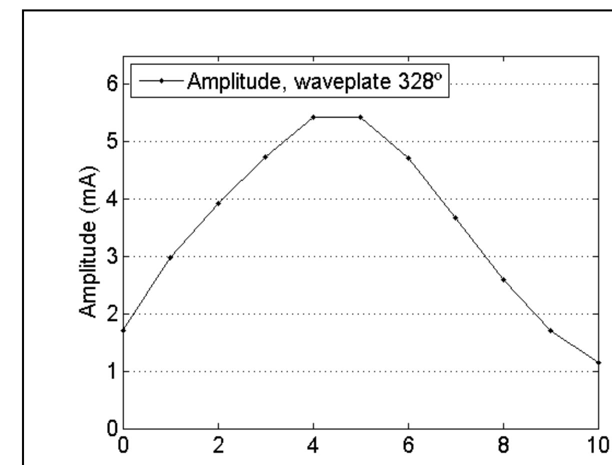

Fig.2. Current peak amplitude as a function of focusing distance with reverse bias of 12V.

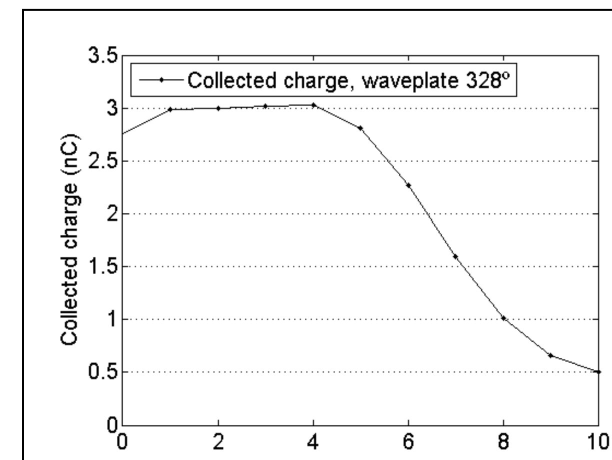

Fig.3. Collected charge as a function of focusing distance with reverse bias of 12V.

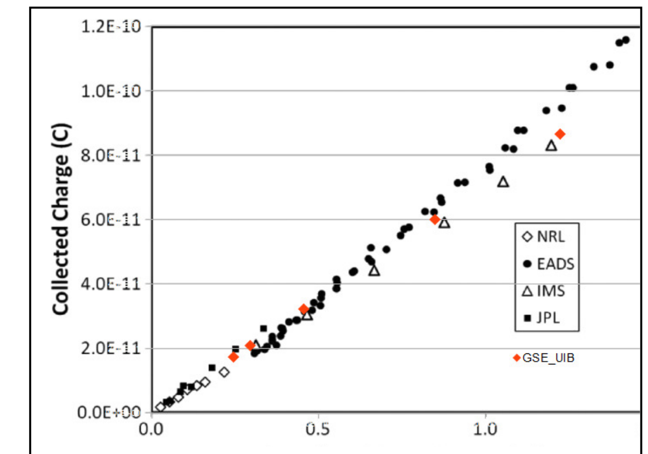

Fig.4. Charge collection at 12V bias as a function of corrected laser energy (data for EADS; IMS, JPL and NRL have been extracted from [1]).

High efficiency interdigitated-back-contact c-Si solar cells

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1. Abstract

In this work we describe a baseline fabrication process of interdigitated-back-contact IBC c-Si(p) solar cells, which combines conventional diffusion oven stages to define base p+ and emitter n+ regions at the back side, with outstanding front surface passivation using atomic layer deposited Al_2O_3 films. Best fabricated device reaches efficiency up to 20.3% (AM1.5G 1 kW/m^2, T=25ºC), with a short circuit density J_{sc}, open circuit voltage V_{oc} and fill factor *FF* of 40.6 mA/cm^2, 648 mV and 77.2% respectively.

2. Introduction

The interdigitated-back-contacted (IBC) solar cell concept is a promising photovoltaic structure for both laboratory and industrial crystalline silicon solar cells [1]. In this kind of cell, both base and emitter contacts are placed at the rear side of the cell, whereas light impinges on the opposite device surface (front side).

Some advantages of this structure are evident, such as the absence of metal shadow losses and the facility to assemble solar cells in modules with coplanar connection. However, in this type of device a high bulk lifetime, outstanding front and rear surface passivation, and low front reflectance are mandatory to obtain high efficiency solar cells. Atomic layer deposition ALD AL_2O_3 process is an excellent technique to achieve both outstanding surface passivation and very low reflectance combined with random pyramids [2] or other surface etching treatments, e.g. black silicon [3].

In the last decade, the Micro and Nanotechnologies Group at the Universitat Politecnica de Catalunya UPC MNT has been developing a baseline process to fabricate high efficiency (~20%) passivated emitter and rear cell PERC cells [4], [5]. In this work, we have adjusted this baseline process to manufacture high performance IBC devices combining conventional oven stages (boron and phosphorous diffusions and thermal oxidations), photolithography and front surface passivation with ALD Al_2O_3 over textured surfaces with random pyramids.

3. Baseline fabrication process and results

IBC solar cells were manufactured using high quality FZ <100> c-Si(p) 4" wafers with resistivity and thickness of 2.5±0.3 Ωcm and 280±20 µm respectively. Cells were fabricated using the flow process shown in Fig. 1, considering next main technological features, namely: 1) boron and phosphorous diffusions to form p+ (base contacts) and n+ (emitter regions) regions respectively, which are patterned using standard photolithography. 2) A front surface textured with random pyramids and passivated with 90 nm ALD Al_2O_3 films, resulting reflectance values below 0.5% at wavelengths λ~600 nm with effective surface recombination velocities below 3 cm/s (@ 1Sun). 3) A back reflector scheme consisting of a thermal SiO_2 (110 nm)/Al (~2 µm) stack was included at the rear side.

A total of 4 solar cells (3 cm × 3 cm area) with different emitter coverage f_e (67%, 75%, 80% and 86%) were fabricated in each wafer (see Fig. 2).

Cells were measured under AM1.5G 1 kW/m^2 solar spectrum (T=25ºC). Photovoltaic parameters are summarized in Table 1. The current-voltage (*J-V)* and power-voltage (*P-V)* characteristics of the best device (cell labelled #4 with f_e=75%) is shown in Fig. 3. Its external quantum efficiency *EQE* and front reflectance *R* curves are plotted in Fig.4. Measurements confirm outstanding efficiencies η's up to 20.3%, with a short circuit current density J_{sc}, open circuit voltage V_{oc} and fill factor *FF* of 40.6 mA/cm^2, 648 mV and 77.2% respectively for the best device. However, 3D simulations envisage even higher efficiency values (>~22%) in future runs using a selective emitter, lower substrate resistivities ~1Ωcm and increasing Al metallization thickness from 2 to 5 µm.

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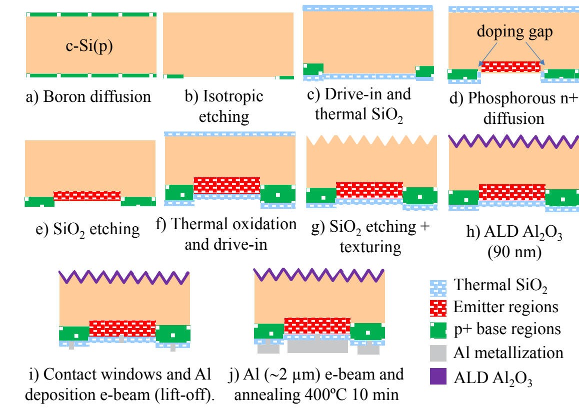

Fig. 1. Main stages of the baseline fabrication process with homogeneous emitter.

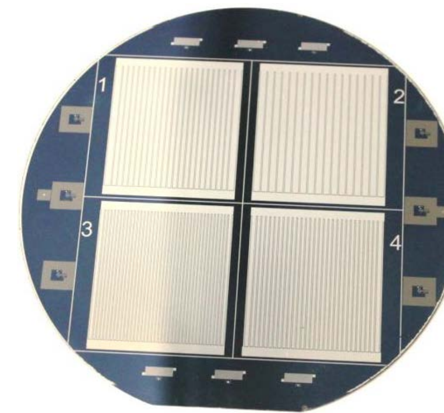

Fig. 2. Back side of a manufacturated wafer showing the four fabricated devices labelled #1, #2, #3 and #4, corresponding to emitter coverage values f_e's of 80%, 86%, 67% and 75% respectively.

Cell	f_e (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)
#2	86	652	41.0	75.0	20.0
#1	80	651	40.9	72.4	19.3
#4	**75**	**648**	**40.6**	**77.2**	**20.3**
#3	67	644	40.0	77.1	19.9

Table 1. Photovoltaic parameters of the fabricated devices. Measurements were performed under standard test conditions STC (AM1.5G 1 kW/m^2 solar spectrum and T=25ºC).

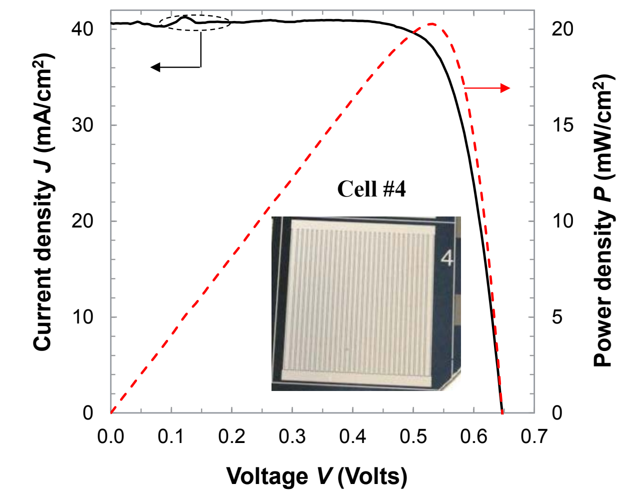

Fig. 3. *J-V* and *P-V* characteristics of the best device (cell #4).

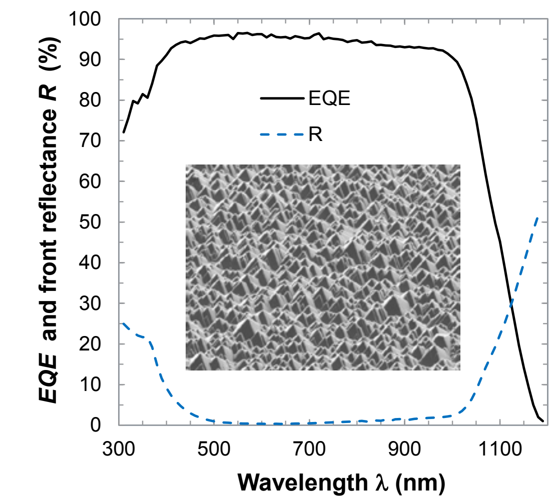

Fig. 4. *EQE* and front reflectance *R* curves of the best device (cell #4). Reflectance was measured in a precursor sample. A SEM image of the textured surface with random pyramids is also added in the inset.

Flexible gas sensing devices with directly grown tungsten oxide nanoneedles via AACVD

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Abstract

Flexible gas sensing devices have been fabricated by directly integrating polymer-based platforms and highly crystalline tungsten oxide nanoneedles grown via aerosol-assisted chemical vapor deposition (AACVD).

The interest in technologies for gas detection based on flexible substrates has increased due to its ability to add new functionalities to devices while reducing production costs. The availability of flexible sensors that include inorganic materials such as semiconductors, will certainly lead to breakthroughs in areas where detection of gases is relevant. Specifically, gas sensors based on semiconductor metal oxides show great advantages because of its sensitivity to a large number of gaseous species and their low costs. Nowadays still remain hard limitations on the quality of semiconductors that can be integrated onto flexible materials due to the high temperatures required for synthesis of these materials. In this sense, some strategies for the integration of semiconductors with flexible substrates have been described in the literature, particularly based on post-transfer methods [1], [2], however, the use of single-step direct vapor-phase methods has not been reported yet. Here, AACVD was used to overcome the temperature restrictions for the integration of nanostructures due to its suitability for generating nanomaterials at low temperatures [3].

In this work, a high heat resistant polyimide foil (Upilex-S, 125 µm, UBE) has been used to fabricate the transducing platforms. The heater was patterned by lift-off process of a Ti/Pt (25 nm/250 nm) film, the insulation layer was deposited on the heater by spin coating of polyimide precursor (U-Varnish, UBE), and after contact opening, the electrodes Ti/Pt (25 nm/250 nm) were patterning following the same procedure used for the heater (Figure 1a). Electrothermal simulations of the heater were carried out using the Joule Heating and Thermal Expansion model of COMSOL Multiphysics 4.3a, and electrical characterizations were achieved using an electrometer (Keithley 2400).

Tungsten oxide nanostructures (Figures 1b and 1c) were grown on the top of the electrodes via AACVD of tungsten hexacarbonyl (40 mg, $W(CO)_6$, Sigma-Aldrich, ≥97%) dissolved in methanol (10 ml, Sigma-Aldrich, ≥99.6%). The morphology of the sensing film was examined using Scanning Electron Microscopy (SEM and EDX — Carl Zeiss, Auriga Series), and the structure (Figure 2) using X-Ray Diffraction (XRD — Bruker, AXS D8- Advance, Cu Kα radiation).

Gas sensors were tested in a continuous flow (100sccm) test chamber provided of mass flow controllers (Brooks 5850E) to regulate the mixture of pure synthetic air and the test gases (C_2H_5OH or H_2, Praxair). Gas sensing tests were carried out for hydrogen (50 ppm) and ethanol (100 ppm) at different operating temperatures from 150 to 250 ºC. Gas sensing tests demonstrated repeatable and satisfactory responses towards ethanol and hydrogen, obtaining the best results at an operating temperature of 250ºC (Figure 3).

Acknowledgment

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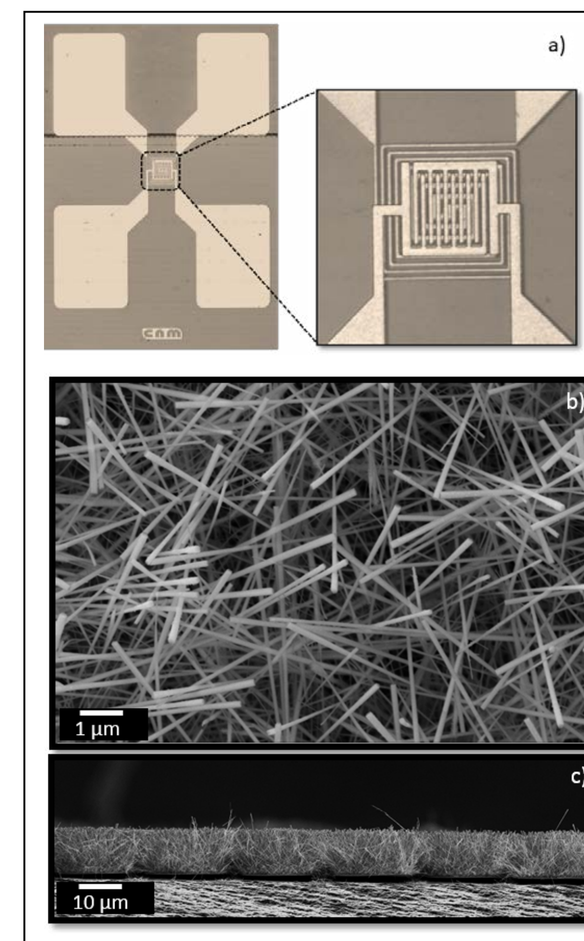


Fig.1. Photograph of the polymeric transducing platform (a). Top view (b) and cross-section (c) SEM images of the nanoneedles integrated on the polymeric transducing platform.

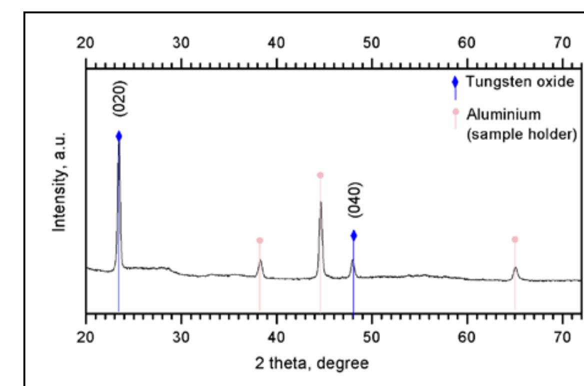
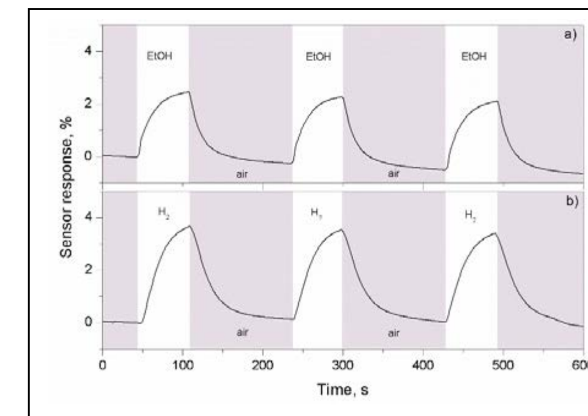


Fig.2. XRD patterns of the tungsten oxide NNs films deposited on polymer-based transducing platforms. Diffraction peaks at 23.5∘ and 48.2∘ 2



Dynamic processes in perovskite solar cells

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Organometal halide perovskite-based solar cells have recently realized large conversion efficiency over 19% showing great promise for a new large scale cost-competitive photovoltaic technology. The proficient operation of the CPbX3 perovskite solar cell, where C is an organic cation, has been accomplished by many different approaches, and it points to a robust photovoltaic operation mechanism that so far has not yet been fully understood. We report the behaviour of lead halogenate perovskite solar cell probed by a number of dynamic techniques including impedance spectroscopy and time transient dynamics. We compare a number of compositions and morphologies and we show the general characteristics of the observed processes. New and interesting phenomena govern the solar cell behaviour in the long time scale, that influence the solar cell performance in phenomena as hysteresis or time dependent luminescence. These results indicate the need for detailed studies to relate structural and electronic behaviours in the perovskite solar cells.

Distinguishing conductive filament and non-localized gate conduction in resistive switching devices

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1. Abstract

A method to separate the localized current through the conductive filament from the non-localized gate current for the low conductivity state of the resistive switching phenomenon is presented. The method uses MOSFETs and it is based in the evaluation of the location of the filament along the transistor channel.

2. Introduction

Resistive switching (RS) phenomenon in Hf based dielectrics provokes the formation of a localized conductive filament (CF) through the dielectric [1,4]. CF conduction can change from a high resistance state (HRS) to a low resistance state (LRS) successively during cycling. However, when at the HRS state, it is difficult to determine if the gate current (I_G) entirely flows through the CF or if the conduction across the whole dielectric area could be relevant. In this work, we demonstrate that the use of MOSFETs allows obtaining more detailed information about the conduction through the CF and through the dielectric area during the HRS.

3. Experimental

The samples were pMOSFETs with FUSI gate (W=0.15 µm, L=0.145 µm and 0.25µm). The dielectric gate stack consists of 1nm SiO_2 and 2.6nm HfSiON. The samples were subjected to the measurement scheme shown in Fig. 1: a Current Limited-Ramped Voltage Stress (CL-RVS) was applied to the gate terminal with the rest of terminals grounded to switch to the LRS (Set process) under current limited conditions, and a Ramped Voltage Stress (RVS) without current limit to switch to the HRS (Reset process). The transistor characteristics of the sample before and after each cycle were registered to evaluate the oxide damage and CF location. The location of the CF along the transistor channel (α) has been defined as $\alpha = I_D/(I_D+I_S)$ [1]. Values of α close to 1 (0) mean CF location near the drain (source) [5].

4. Discussion

Fig. 2 shows the typical I_G behavior during voltage cycling. The transition from HRS to LRS (left) occurs when the gate voltage reaches the Set voltage (V_{SET}) and a sudden increase of I_G is produced. The change from LRS to HRS (right) takes place at some Reset voltage (V_{RESET}) and the current drops several orders of magnitude reaching a lower conductive state (HRS state). The change between the HRS and the LRS can be obtained successively if the sequence of Fig. 1 is repeated. Two locations of the CF, close to the source/drain respectively were studied. Fig.3(top) shows the value of α in a sample at the LRS after successive SET events. Since at the LRS, I_G is controlled by the CF current (I_{CF}) and $\alpha\sim 0$ means that the CF is located close to the source. Fig. 3 (bottom) shows α obtained for the HRS during cycling as a function of I_G. For the larger I_G values, α is very close to 0. However, lower I_G corresponds to α values closer to 0.5. These results can be interpreted considering that the total I_G is divided in two components, one related to the CF conduction itself (I_{CF}) and the other one to the non-localized conduction through the rest of the area of the device (I_{NLC}) (Fig.4). When the CF conduction is relevant (larger I_G values) I_{CF} dominates and I_{NLC} becomes negligible, which explains the α values close to 0 for the HRS. However, for lower values of I_{CF}, the filament can be considered 'closed' and I_{NLC} becomes relevant. As I_{NLC} is distributed through the transistor area, the portion of this current that is collected at the drain and source terminals tends to be the same, which explains α values larger than 0 (Fig. 3 bottom). This explanation is supported by the fitting of the experimental curve (line in Fig. 3 bottom) by the formula: $\alpha=0.5I_{NLC}/I_G$, (eq.1). I_{NLC} is a fixed parameter obtained by least squares. Considering that $I_G=I_{CF}+I_{NLC}$, then the formula can be rewritten as $\alpha=0.5I_{NLC}/(I_{CF}+I_{NLC})$, (eq.2). This allows to obtain separately I_{NLC} and I_{CF} and consequently to obtain more accurately the current through the filament for the HRS. Fig. 5 (top) shows the case of CF location close to the drain ($\alpha\sim1$) for the LRS during cycling in another sample. Fig. 5 (bottom) shows α obtained after the Reset events during cycling as a function of I_G. The fitting of the curves is obtained with the expression: $\alpha=(I_G-0.5I_{NLC})/I_G$ (eq.3). I_{NLC} increases with cycling, which suggests degradation of the whole dielectric area with cycling. Considering again $I_G=I_{CF}+I_{NLC}$ the formula can be rewritten as: $\alpha=(I_{CF}+0.5I_{NLC})/(I_{CF}+I_{NLC})$ (eq.4) which allows to obtain I_{CF}.

5. Conclusions

A method to separate the localized current through the CF from the non-localized gate current for the HRS using MOSFETs is presented. The method is based in the determination of the location of the CF along the transistor channel and can help to analyze the CF conduction properties in RRAM devices.

Intrinsic factors determining the metal-graphene contact resistance

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1. Abstract

The resistance of the metal-graphene contact is a technological bottleneck for the realization of viable graphene electronics, including radio-frequency devices. Despite the large number of experimental works in the existing literature measuring the contact resistance, a big effort is still needed to unveil the intrinsic and extrinsic factors determining it. In this work we present a comprehensive model, based on a combination of the Bardeen Transfer Hamiltonian method with the Landauer formula to find the components of the contact resistance determined by the sequential tunneling of carriers between the metal and graphene underneath followed by Klein tunneling to the graphene in the channel. This model unveils the role played by different electrical and physical parameters in determining the contact resistance, such as the chemical potential of interaction, the metal-graphene work function difference, the metal-graphene equilibrium distance, the gate capacitance and the temperature.

While graphene has emerged as a promising material for future electronic devices thanks to its unique electronic properties, the metal-graphene contact resistance (Rc) remains a limiting factor for graphene-based electronic devices [1]. In particular, for high frequency electronics is an issue, very much influencing figures of merit like the maximum frequency of oscillation, the cutoff frequency, or the intrinsic gain [2]. That is why there is aneed to understand the intrinsic and extrinsic factors determining the contact resistance, which displays a strong variation depending on the metal contact and fabrication procedure details [3-5]. To gain understanding of the intrinsic factors a comprehensive physics based model of the contact resistance is worthy. One relevant model was already proposed by Xia et al. to describe the transport in metal-graphene junctions as a sequential tunneling process from the metal to graphene underneath followed by injection to the graphene channel [6]. The first process is responsible for the resistance between the metal and the graphene underneath (Rmg) and the second process includes the resistance due to the potential step across the junction formed between the graphene under the metal and the graphene channel (Rgg). The total contact resistance is then the series combination of both contributions, Rc = Rmg + Rgg. However, there is an important ingredient determining Rc namely, the transmission from a 3D system (metal) to a 2D system (graphene), that was not properly considered in a physics basis. So, in order to improve the state-of-the-art and current understanding, we have taken this issue of the carrier transmission from 3D to 2D systems into consideration. Specifically, we have developed a physics-based model where the calculation of Rmg and Rgg are based on the Bardeen Transfer Hamiltonian (BTH) method [7-8] and the Landauer approach [9], respectively. The BTH method allows us to get information about the matrix elements for the transition between 3D-metal and 2D graphene states and combined with Fermi's golden rule, yields a compact expression for the specific contact resistivity. On the other hand, the Landauer approach allows to get the conductance of carriers across the potential step between the graphene under the metal and the graphene in the channel, where the angular dependence transmission of fermions have been taken into account.
For the calculation of Rc we have considered both the gate voltage and temperature dependence considering a FETdevice. As an illustrative example of our model outcome we show in Fig. (1) the calculated specific contact resistivity of the metal-graphene junction for different metal electrodes together with Fig. (2) showing the contact resistance with Palladium as metal electrode. These theoretical predictions match pretty well with experimental data from different authors, and in particular with Ref. [6].

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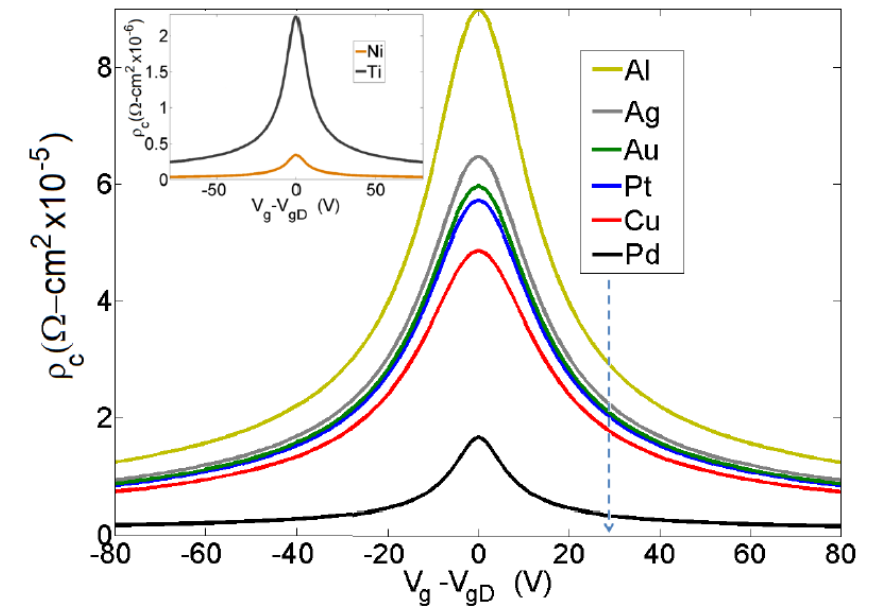

Fig. 1. Specific contact resistivity for different metal electrodes centered at the Dirac gate voltage VgD.

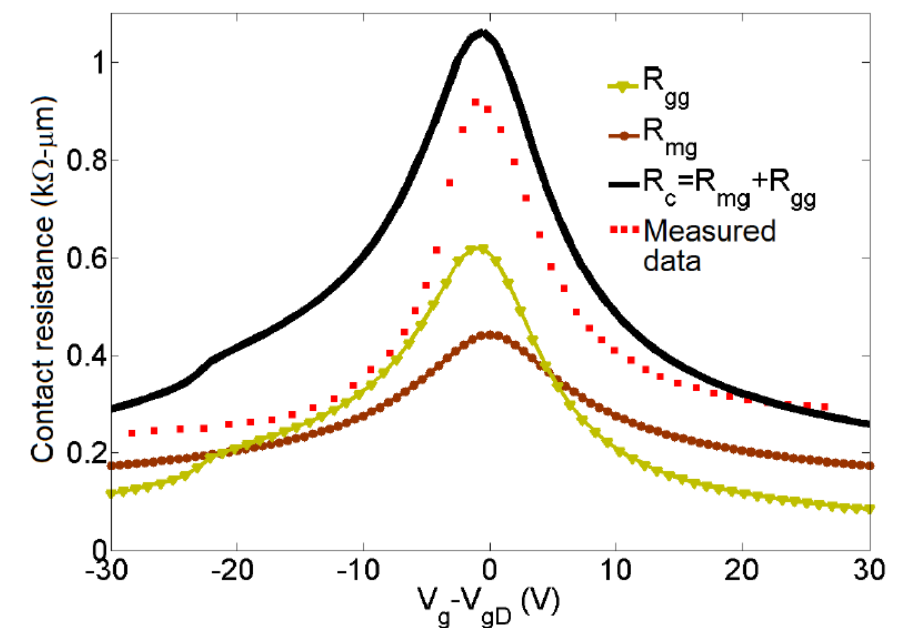

Fig. 2. Contact resistance as function of the back-gate bias overdrive for Pd as metal electrode. Experimental data arefrom Ref. [6].

Modeling of the *I-V* and *I-t* Characteristics of Multiferroic $BiFeO_3$ Layers

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1. Abstract

We have investigated the current-voltage (*I-V*) and current-time (*I-t*) characteristics of $Pt/BiFeO_3/SrRuO_3$ structures fabricated on $SrTiO_3$ substrates. The devices exhibit resistive switching effect under the application of a single and multiple voltage loops. The *I-V* curves are simulated using a Schottky-like conduction model with varying parameters. The model includes series resistance correction and barrier lowering. The *I-t* curves are fitted using a power-law model. It is found that the Schottky barrier height (SBH) modulation arising from the $BiFeO_3$ polarization reversal is remarkably lower (<0.07 eV) than previously reported (>0.5 eV) and that the current decay for a constant applied voltage is characterized by very small power exponents ($\sim10^{-2}$).

2. Introduction

Recent studies have shown that multiferroic $BiFeO_3$ (BFO) is a promising material for the next generation of nonvolatile memory devices because of its resistive switching (RS) properties [1]. Structures based on this material do not require electroforming, exhibit rectifying and tunable conduction characteristics, and show high endurance and data retention [2]. The ON (high current) and OFF (low current) conduction states are related to the polarization reversal property exhibited by the BFO film when subjected to opposite electric fields. Several models have been proposed to account for the *I-V* characteristics of these devices: space charge limited conduction, Poole-Frenkel, tunneling and Schottky-like conduction [3]. Here, a compact representation for the minor and major *I-V* loops in $Pt/BFO/SrRuO_3$(SRO) structures is reported. We also show that when in the ON state, the devices show some instabilities for positive applied biases.

2. Results and Discussion

The devices under investigation are Au(100nm) /Pt(10nm)/BFO(100nm)/SRO(50nm)/SrTiO3 structures. The SRO bottom electrode was grown on the substrate prior to a pulsed laser-deposited BFO layer. Both the BFO and SRO layers were epitaxially grown. The Au/Pt top electrode was deposited on the BFO layer through a shadow mask by E-beam evaporation. More details about the fabrication and characterization of the Bi-deficient BFO films investigated in Ref.[1]. The *I-V* characteristics are simulated using the Schottky model:

$$I(V) = AA^*T^2\exp(-\phi_B/kT)\{\exp[e(V-IR_S)/nkT]-1\} \quad (1)$$

where A is the device area, A^* the effective Richardson constant, T the temperature, e the electron charge, k the Boltzmann constant, R_S the series resistance and n the ideality factor. ϕ_B is the effective barrier height $\phi_B=\phi+\beta V H(-V)$, where ϕ is the SBH, $\beta>0$ a constant, and H the step function. The fraction of downward polarized domains $0\leq\lambda\leq1$ is given by the expression:

$$\lambda(V)=1/\{1+\exp[-r(V-V_S H(\dot{V})-V_R H(-\dot{V}))]\} \quad (2)$$

where r is the switching rate, V_S the set voltage and V_R the reset voltage. The dot corresponds to the time derivative. The state of the system is described by the vector $\Omega=(I_S,\alpha,R_S)$ which follows the parametric relationship:

$$\Omega=\Omega_m+\lambda(\Omega_M-\Omega_m) \quad (3)$$

We define $I_S=AA^*T^2\exp(-\phi/kT)$ and $\alpha=e/nkT$. Ω_m and Ω_M are the minimum and maximum of Ω, respectively. Figures 1 and 2 show simulation and experimental results using (1)-(3). The SBH modulation is calculated from the reverse current as $\Delta\phi=kT\ln(I_{SM}/I_{Sm})$. For the curve illustrated in Fig.1, $\Delta\phi\approx0.07$ eV is obtained which is far lower than previously published values: 0.6 [4], 1.38 [5], 0.5 eV [6]. The *I-t* curves can be described by a power-law model (see Figs.3 and 4):

$$I(t)=at^{-b} \quad (4)$$

where a and b are positive constants. This current decaying law has often been associated with relaxation and degradation mechanisms of dielectric films in capacitors (Curie-Von Schweidler law). Similar parameter values to those found in this work ($b\sim10^{-2}$) have been obtained for BFO in [7,8], however understanding the physical connection of (4) with the BFO partial polarization reversal still requires further investigation.

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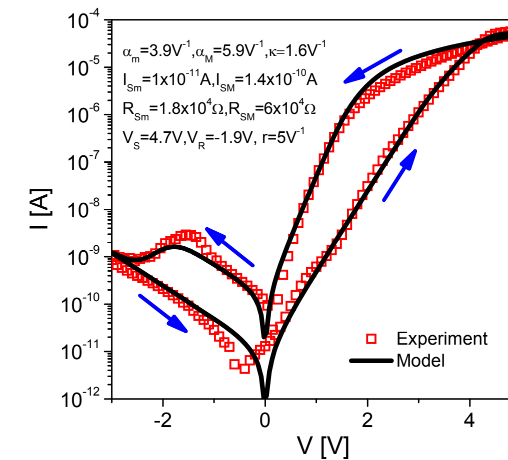

Fig. 1- Experimental and simulated I-V charcteristics using eqns(1)-(3). Major loop.

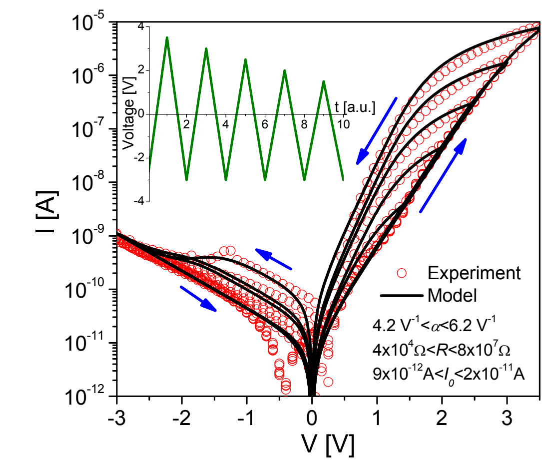

Fig. 2- Experimental and simulated I-V charcteristics using eqns(1)-(3). Minor loops.

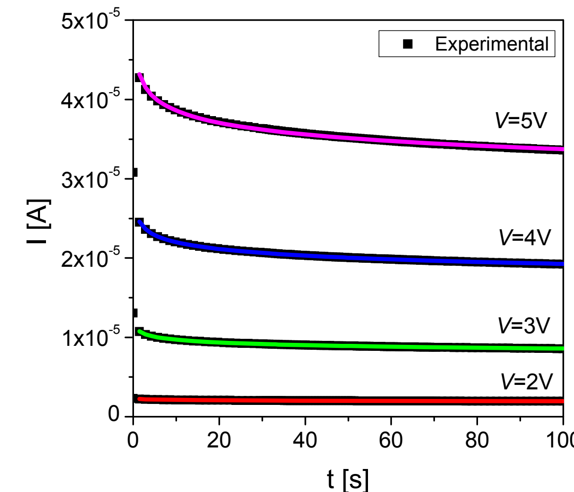

Fig. 3- Experimental and simulated I-t chracteristics using eqn(4). Linear-linear plot.

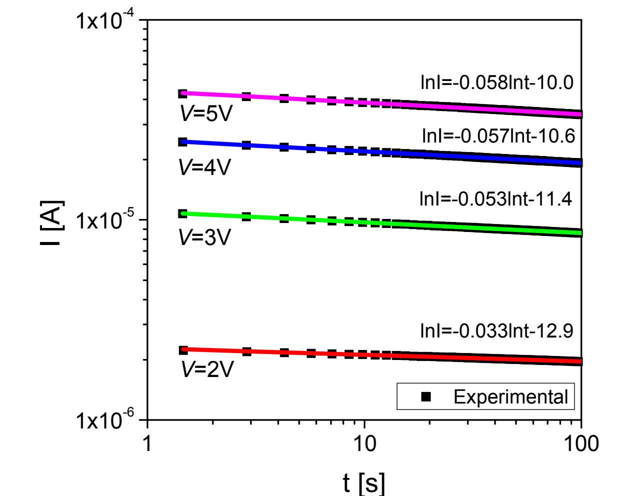

Fig. 4- Experimental and simulated I-t chracteristics using eqn(4). Log-log plot.

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RADFET response to photon and electron beams

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1. Abstract

A comparative study of Radiation-sensitive field effect transistors (RADFETs) response to photon and electron beams has been carried out in reference conditions. Both types of beams, routinely used in clinical radiotherapy, have been applied to RADFETs of several gate oxide thicknesses, sizes and technological processes manufactured by Tyndall National Institute, showing very similar responses in terms of sensitivity and linearity with dose ranges typical of clinical radiation treatments.

2. Introduction

RADFETs have oxides optimized in order to increase the radiation sensitivity. Radiation-induced trapped holes produce in the RADFET a threshold voltage shift, ΔV_T, which is used to measure the absorbed dose in the oxide, *D*. It is known that the dependence of the voltage shift with the dose follows a power law relationship [1]:

$$\Delta V_T = A \cdot D^n \quad (1)$$

where $\Delta V_T = V_T - V_{T0}$, with V_{T0} and V_T is the threshold voltage before and after irradiation, respectively, and *A* and *n* are fit parameters.

3. Materials and methods

The experimental samples were Al-gate p-channel MOS transistors manufactured by the Tyndall National Institute (Cork, Ireland). Gate oxides of 100 nm, 400 nm and 1µm were grown as pure thermal oxides (100 nm and 400nm) or a combination of thermal and CVD oxide (1µm). Three types of 400 nm device were tested in this work (400 nm_W5, 400 nm_W7 and 400 nm_W8). 400 nm_W5 can be called a "standard" process; 400 nm_W7 and 400 nm_W8 are identical to the standard process, except for higher post-oxidation anneal temperature and duration. Each chip contained four individual RADFETs, organized as two pairs with unique geometry. The linear accelerator Mevatron KDS (Siemens, Berlin, Germany) placed at the Hospital Universitario "San Cecilio" in Granada (Spain) was employed to irradiate RADFETs with 6 MV photon and 6 MeV electron beams. To measure the V_T increment with the dose, the portable dosimetry system developed by Carvajal et al. [2] was used. The response to radiation was analysed with a threshold voltage shift equal to the source voltage shift at constant I_{ZTC} drain current, thus reducing the temperature effect. In all cases, experimental data have been fitted to the potential model given in Eq. 1.

4. Results and discussion

In Fig. 1, the accumulated V_T shift versus the dose for the type with 100 nm oxide of both sizes (W/L= 300/50 and 690/15 µm) are plotted and fitted to Eq. 1. We also studied the response of different type of RADFETs with 400 nm and 1 µm of gate oxide thickness (Fig. 2 and 3). Table 1 lists the parameters *A* and *n*, for the calibration curves of the different studied RADFETs. Generally speaking, in all the studied cases there is a sub-linear behaviour, n<1, mainly due to the electric field screening produced by the radiation-induced oxide charges. Moreover, the *A* parameter increases and *n* decreases with the gate oxide thickness for both ionizing sources in accordance with others experimental studies with photon beams [3,4]. Bigger sensitive volumes provide higher *A* values due to higher radiation-induced oxide charge which enhances the electric field screening in the oxide, decreasing the exponent *n*.

To sum up, experimental results demonstrate that the response of RADFETs in electron beams is very similar, within experimental uncertainty, to photon beams in reference conditions.

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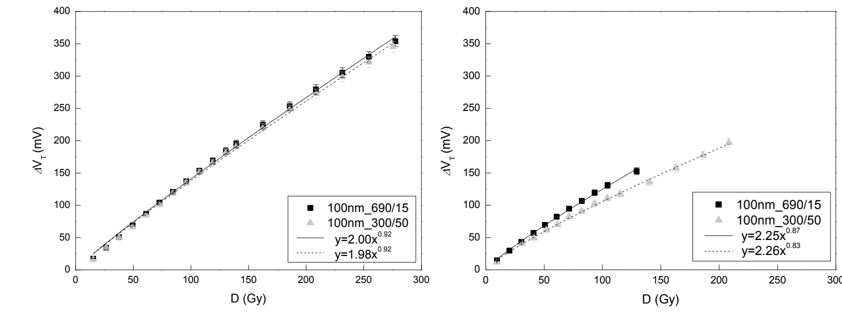

Fig. 1. ΔV_T vs. *D* of RADFETs with t_{ox} = 100 nm and W/L = 300/50 and 690/15, irradiated with photon (left) and electron (right) beams.

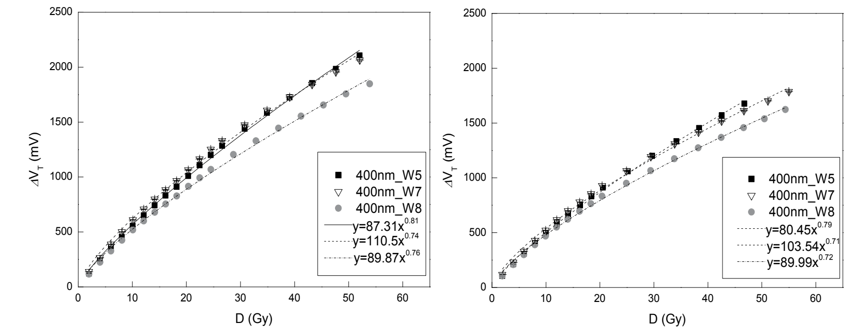

Fig. 2. ΔV_T vs. *D* of RADFETs of t_{ox} = 400 nm, with W/L = 300/50, irradiated with photon (left) and electron (right) beams.

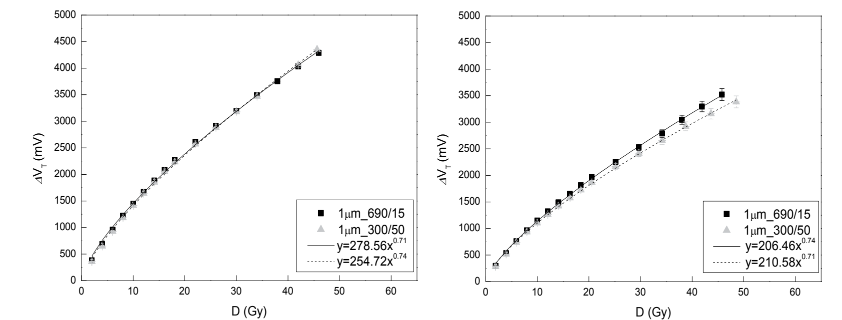

Fig 3. ΔV_T vs. *D* of RADFETs (t_{ox} = 1 µm and W/L = 300/50 and 690/15), irradiated with photon (left) and electron (right) beams.

Type	Size (W/L)	Photon Beam		Electron Beam	
		$\Delta V_T = A \cdot D^n$			
		A	n	A	n
100 nm	**300/50**	2.0 ± 0.3	0.91 ± 0.03	2.2 ± 0.3	0.83 ± 0.03
	690/15	2.03 ± 0.19	0.92± 0.02	2.2 ± 0.3	0.87 ± 0.03
400 nm_W5	**300/50**	91 ± 5	0.80 ±0.01	79 ± 3	0.79 ± 0.01
	690/15	81 ± 4	0.83 ± 0.01	83 ± 6	0.78 ± 0.02
400 nm_W7	**300/50**	113 ± 8	0.74 ±0.02	104 ± 6	0.73 ± 0.01
	690/15	103 ± 5	0.77 ± 0.02	105 ± 6	0.72 ± 0.01
400 nm_W8	**300/50**	73 ± 11	0.81 ±0.05	79 ± 10	0.73 ± 0.01
	690/15	86 ± 10	0.77 ± 0.02	85 ± 7	0.73 ± 0.01
1 µm	**300/50**	240± 20	0.76 ± 0.02	213 ± 9	0.72 ± 0.01
	690/15	250 ± 50	0.74 ± 0.04	202 ± 9	0.74 ± 0.01

Table 1. Fitting parameters of RADFET response according to the potential model for every size and type for photon and electron ionizing radiation. ΔV_T was expressed in mV and *D* in Gy.

Effect of doping in the current voltage characteristics of Organic diodes

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1. Abstract

We analyze the effects of doping, traps and other defects on the electronic properties of organic/polymeric diodes. We detect the presence of dopant atoms and traps in the semiconductor in experimental current density-voltage (*j-V*) curves by the comparison with numerical *j-V* curves. The transport equations are solved by means of the Lambert-W-function. The key parameter in the procedure is the boundary value for the free carrier density at the metal-organic interface.

2. Motivation

Dopant impurities, traps and defects can be introduced in organic devices in a controlled way during the fabrication process, or they can appear by degradation of the devices due to ambient contaminants. Important figures-of-merit of the devices are strongly affected by the trapping of charge [1],[2],[3]. In this work, we propose a way to detect their presence in the semiconductor by analyzing the value of the free charge density at the metal-organic interface [4],[5].

3. Procedure and Results

In organic diodes with symmetric contacts, the free charge carriers $p_f(x)$ (holes in a hole-only device) move through the bulk of the organic material mainly by the action of an electric field $F(x)$ according to:

$$j = qp_f(x)\mu F(x) \tag{1}$$

where q is the value of the electron charge, x is the distance from the electrode, μ is the carrier mobility and j is the current density. The existence of traps contributes to increase the amount of fixed charges, p_t, in the semiconductor. The total charge density qp is the sum of free qp_f plus fixed qp_t charges densities, and is related to the electric field F by the Poisson's equation:

$$\frac{dF(x)}{dx} = \frac{q}{\varepsilon_0\varepsilon_r}\left(p_f(x) + p_t\right) \tag{2}$$

where ε_r and ε_0 are the relative permittivity and free space permittivity, respectively. Combining equations (1) and (2), the following relation is obtained:

$$\int_{F(0)}^{F(x)} \frac{\mu\varepsilon_0\varepsilon_r F dF}{j + qp_t\mu F} = \int_0^x dx \tag{3}$$

The set of transport equations is completed with the integral of the electric field to find the voltage along the device of length L:

$$V = \int_0^x F(x)dx \tag{4}$$

In order to extract *j-V* (current density-voltage) curves, equations (1)-(4) can be solved numerically. Fortunately, a semi-analytical solution is found when the mobility is considered as a constant value. Applying the exponential function to the two parts of (3) and multiplying by $-e^{-1}$, the following expression is obtained:

$$\begin{aligned} &Ye^Y = X \\ &Y = -\left(1 + qp_t\mu F(x)/j\right) \\ &X = -\left(1 + qp_t\mu F(0)/j\right)\exp\left[-\left(1 + qp_t\mu F(0)/j\right)\right]\times \\ &\exp\left[-x\left(qp_t\right)^2\mu/\left(\varepsilon_0\varepsilon_r j\right)\right] \end{aligned} \tag{5}$$

This equation can be solved by using the Lambert W-function Y=W(X) [6]. Then, the electric field is:

$$\begin{aligned} &F(x) = -j/(qp_t\mu)\times \\ &\{1 + W[-\left(1 + qp_t\mu F(0)/j\right)\times \\ &\exp\left[-\left(1 + qp_t\mu F(0)/j\right) - x\left(qp_t\right)^2\mu/\left(\varepsilon_0\varepsilon_r j\right)\right]]\} \end{aligned} \tag{6}$$

The value of the charge density at the metal-organic interface can be extracted from the comparison of experimental *j-V* curves with this model, equations (4), (6).

We have applied this procedure to experimental data measured on glass/ITO/PEDOT:PSS/LEP/Pd diodes [7] (circles in Fig.1). The fitting with our numerical results (solid line) provides a finite value of $p(0)$ as a function of j (inset in Fig. 1). At low voltages, $p(0)$ is constant and gives information about the trapped charge density $p_t = 10^{14}$ cm^{-3}. When the voltage increases, the charge density increases and a space charge region is formed. The limitation of this model is found at much higher voltages, where an electric field dependent mobility model should be used [4]. This does not affect the accurate values of the trapped charge obtained at low electric fields.

4. Conclusion

We propose a simple way to estimate the presence of impurities and traps in organic diodes by comparing experimental *j-V* curves with numerical results. The numerical *j-V* curves are obtained by solving the transport equations with the use of the Lambert W-function. The use of this function requires some assumptions such as constant mobility or constant doping concentration. Nevertheless, accurate values are obtained.

Acknowledgments

This work was supported by Ministerio de Educación y Ciencia under research Grant FPU12/02712, Project mP_TIC_5 from Campus de Excelencia Internacional BioTic Granada and the Canada Research Chair program.

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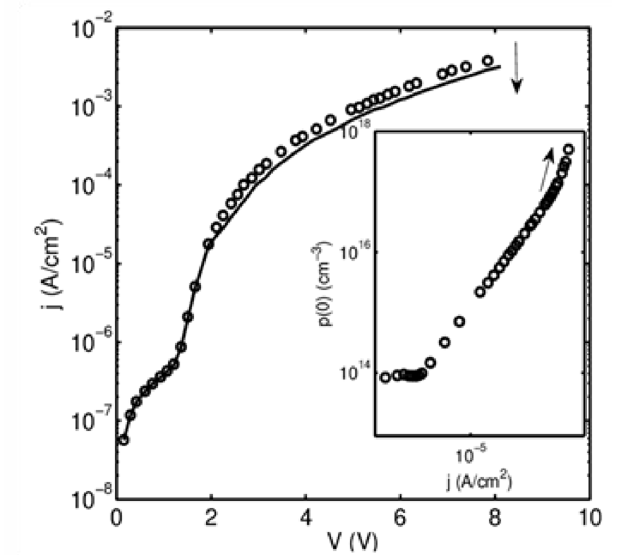

Fig. 1. Comparison of experimental *j-V* curves measured at 295 K in a glass/ITO/PEDOT:PSS/LEP(L = 122 nm)/Pd diode [5] (symbols) (ε = 3.2) with our model, equations (4), (6) (solid line). In the numerical results, μ = 1.28×10^{6}cm^2/Vs and p_t = 10^{14} cm^{-3} are used as fitting parameters. Inset: free charge density at the metal-organic interface extracted with our procedure and employed as a boundary condition in the semi-analytic analysis.

Comparative study of printed capacitive sensors

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1. Introduction

In this work, we will show the design, fabrication and characterization as humidity sensor of four different coplanar electrodes, comparing and contrasting their characteristics. In this regard, we present the design, fabrication and characterization of a capacitive humidity sensor which uses the flexible substrate as sensitive element [1]. These capacitors have been printed with silver nanoparticles by inkjet-printing on a polyimide thin film. In this context, this paper discusses planar printed capacitive sensors in terms of their sensitivity to relative humidity taking into account frequency dependencies. Further investigations of the sensor designs have been carried out using a numerical method.

2. Fabrication process

The DMP-2831™ Dimatix printer (Fujifilm Dimatix Inc, Santa Clara, USA) was used for inkjet printing. The selected materials were an ink of silver nanoparticles (U5603 SunTronic Technology, San Diego, USA) on a polyimide substrate (Kapton® HN with 75 µm of thickness, Dupont™) whose electrical permittivity is directly related to the relative humidity. The fabrication time is much lower than in the case of other sensors because no other sensing layer was needed [2-4] and also because it only required printing one layer on one side of the substrate. In a previous work, we demonstrated that the layer thickness does not contribute significantly to capacitance and therefore the definition of electrodes by only one printed layer is enough for a proper sensor performance [1].

3. Characterization

The physical characterization of the patterns has been carried out using a Dektak XT™ Stimulus Surface Profiling System (Bruker Corporation, Conventry, UK). The electrical characterization has been carried out by measuring their impedances, using the four-wire measurement technique with a Impedance Analyser 4294A and an impedance probe kit (4294A1) (Agilent Tech., Santa Clara, CA, USA). The stationary humidity and temperature responses of the sensors have been measured in a climatic chamber VCL 4006 (Vötsch Industrietechnik GmbH, Germany).

4. Results

Figure 1 illustrates all studied configurations. First, interdigitated electrodes (IDE) have been studied. This structure is the most common one to develop capacitive sensor thanks to its compromise between ease of manufacturing and performance. Then, a periodic electrode structure as a combination of meandering and interdigitated electrodes in a serpentine-shaped geometry in a single structure has been designed, known to us as serpentine electrodes (SRE). Another developed structure uses spiral electrodes which are placed as a coil inductor. Finally, a structure with meandered electrodes is presented. As there are differences in area, we have normalized the found sensitivities to the area of each capacitive sensor. Figure 2 shows the comparison of the sensitivity to relative humidity of each sensor as a function of frequency. All sensors show a similar trend in frequency, with relative higher values at lower frequencies and a sensitivity that tends to a constant value at higher frequencies. In terms of performance, SRE shows the highest sensitivity values, followed by spiral electrodes and IDE. Meandered electrodes present the lowest value. Depending on the specific application and its requirements, we could choose a configuration or another. For example, SRE and spiral electrodes should be selected when sensitivity is a critical factor. But these two designs are more complex than the other two and, therefore, their yield rates are lower than the other two configurations.

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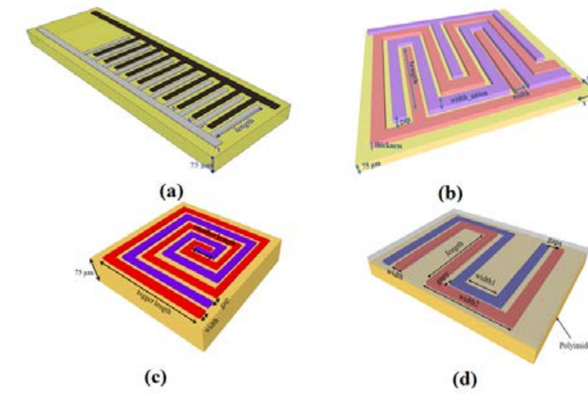

Fig.1. Electrode configurations (a) interdigitated electrodes; (b) serpentine electrodes; (c) spiral electrodes; (d) meandered electrodes.

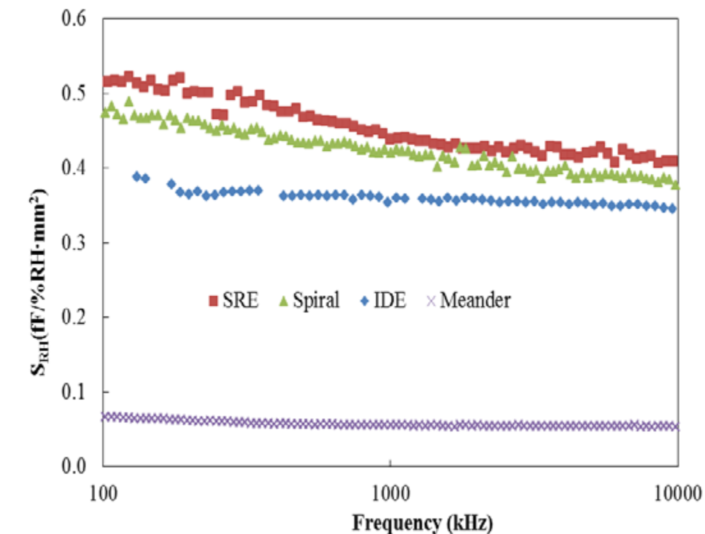

Fig.2. Sensitivity to RH as a function of frequency for each electrode configuration.

Investigation of the Resistive Switching Behavior in Ni/HfO_2-based RRAM Devices

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1. Abstract

In this work, a systematic study of the electrical properties and the cycle-to-cycle variability in Ni/HfO_2-based RRAM devices is presented. Besides the resistive switching behavior, attention is also given to the thermal stability of the conductive filaments.

2. Introduction

Filamentary resistive random access memories (RRAM) based on metal-insulator-metal (MIM) configurations are widely being explored as emerging non-volatile memory devices because of their high scalability, improved switching speed, low power consumption, and potential for 3-D integration. However, switching variability is one of the important problems to be overcome before their industrial application [1-3]. This problem is associated to the instabilities of the switching parameters (currents and voltages) due to the random nature of the reversible conductive filament (CF) formation. Hence, understanding the key mechanisms involved in switching variability is crucial to optimize the device performance and to foster the development of this emerging technology.

3. Experimental

The studied Ni/HfO_2/Si devices were fabricated on (100) n-type CZ silicon wafers with resistivity (0.007-0.013) Ωcm following a field isolated MIS process. The 20nm-thick HfO_2 layer was deposited by atomic layer deposition at 225ºC using TDMAH and H_2O as precursors. The top metal electrode, consisting of a 200nm-thick Ni layer, was deposited by magnetron sputtering. The resulting structures are square cells of 5x5μm^2. A schematic cross-section of the final device structure is shown in the inset of Fig. 1(b). The current-voltage (I-V) measurements were performed using a HP-4155B semiconductor parameter analyzer. The voltage was applied to the top Ni electrode, while the Si substrate was grounded. In order to evaluate the cycle-to-cycle variability, numerous cycles and measurements are necessary to be assessed. For this purpose, a software tool has been developed (implemented by Matlab) to control the instrumentation and to smartly detect the SET and RESET currents.

3. Results and Discussion

Fig.1 shows the nonpolar switching behavior of the studied devices. The unipolar switching phenomenon in Ni/HfO_2/Si devices has been recently analyzed by real time TEM micrographs [4], where it was found that during the SET process, Ni diffusion from the top electrode through the dielectric was detected, leading to the formation of Ni-based CFs. During the RESET process, a partial dissolution of the CFs has been observed due to thermally enhanced diffusion induced by joule heating [4,5]. To analyze the cycle-to-cycle variability [2] associated to Ni diffusion and migration processes in Ni/HfO_2-based RRAM devices, the stability of the switching parameters during successive measurements is evaluated. Fig.2 shows the evolution of the on (I_{on}) and off (I_{off}) state currents at fixed bias (V = -0.2V), corresponding to more than 3000 cycles. In the case of the I_{off} a larger spread of the current values is observed. This fact can be explained by the cyclical variations of the gap distances in the dissolved CF. The evolution of I_{on} versus applied voltage and cycle number is shown in Fig.3, where slight current variations during cycling are evidenced for all the voltages assessed. Additional parameters affecting the device variability are the SET/RESET voltages, V_{set} and V_{reset}, respectively. Fig.4 shows the cumulative distribution functions (CDF) of the V_{set} and V_{reset}. The nearly parallel CDF slopes indicate similar widths of the switching voltages distributions. Besides the cyclical variability, the impact of temperature on the switching stability is also analyzed. It can be observed in Fig.5 that the current obtained for the low resistive state significantly increases with the temperature, suggesting the contribution of tunneling-based transport mechanisms associated to a filament with a narrow constriction [5]. A detailed analysis of the thermal dependence of the switching parameters will be given at the conference.

4. Conclusions

The switching phenomenon of Ni/HfO_2-based devices is investigated. The results show a non-polar resistive switching behavior of the studied 5x5μm^2 devices. Moreover, the cyclical variably is analyzed, where a larger dispersion of the off state current is evidenced. This larger dispersion could be attributed to the cyclical variations of the gap distances. Finally, the electrical and thermal stability of the conductive path is also discussed.

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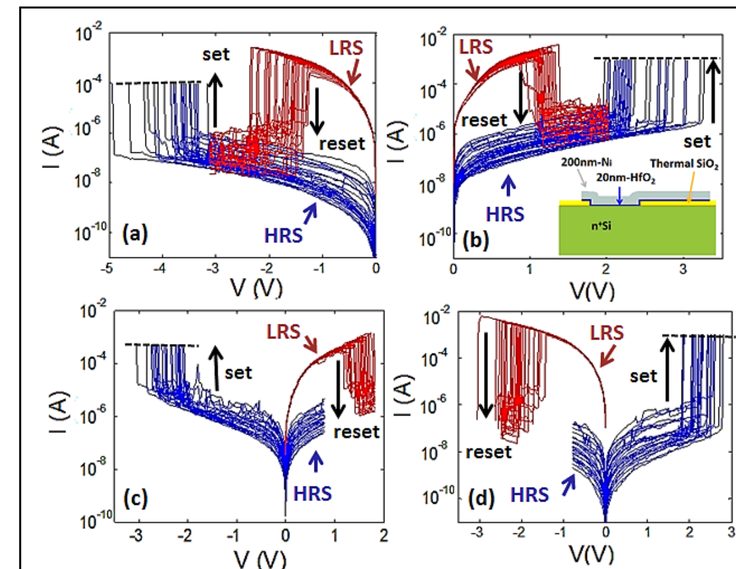

Fig.1. (a)-(d) Nonpolar resistive-switching behavior of Ni/HfO_2-based devices during SET and RESET operations for the different voltage polarity combinations. The inset of Fig. 1(b) shows a schematic cross-section of the studied devices. The area of the devices is 5x5 μm^2.

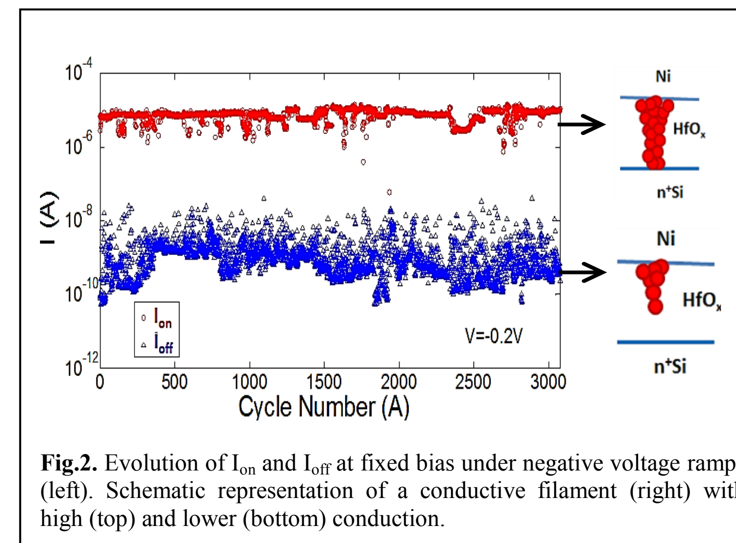

Fig.2. Evolution of I_{on} and I_{off} at fixed bias under negative voltage ramps (left). Schematic representation of a conductive filament (right) with high (top) and lower (bottom) conduction.

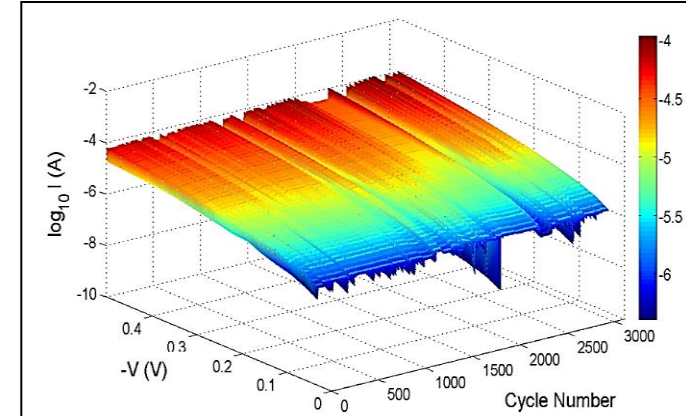

Fig.3. 3-Dimensional plots of I_{on} versus applied voltage and cycle number corresponding to Fig.2.

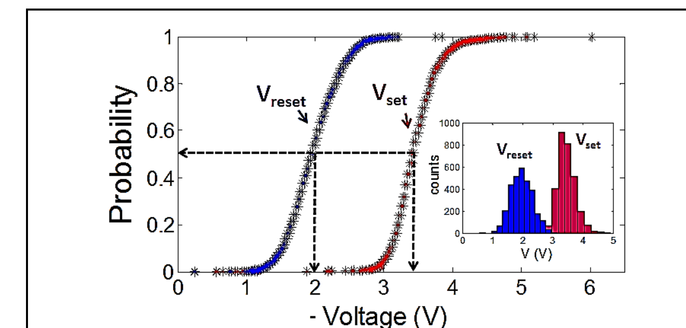

Fig.4. CDF of V_{reset} and V_{set} corresponding to more than 3000 cycles under negative voltage ramps. The inset shows the associated histogram.

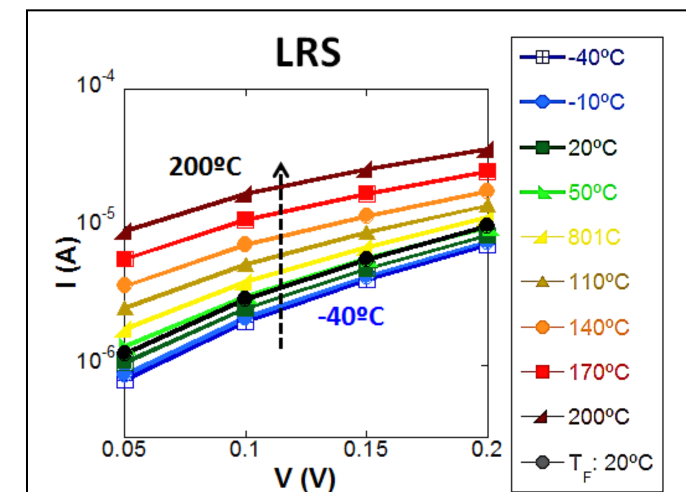

Fig.5. Current-voltage characteristics of the on-state-current for temperatures ranging from -40ºC to 200ºC.

Effect of the blistering of ALD Al_2O_3 films on the silicon surface in Al-Al_2O_3-Si structures

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1. Abstract

Blistering of 11 nm and 45 nm-thick Al_2O_3 layers deposited by ALD on silicon substrates is studied for Al-Al_2O_3-Si structures fabricated using a field isolated process. Blisters are shown to be unevenly distributed and with different dimensions. After chemical etching down to silicon, round voids are revealed underneath the blisters.

2. Introduction

Atomic Layer Deposition (ALD) of Al_2O_3 layers on silicon has attracted increasing attention. Among different applications, it has been shown that Al_2O_3 films are of interest for surface passivation in crystalline silicon solar cells [1,2]. In this technology, high-temperature processes after the oxide deposition are carried out which may cause blistering of the layer [3]. This phenomenon can prevent the use of the layers, particularly when the blister height is large and photolithography steps are necessary. We have already reported [4] a thorough analysis of the conditions under which blistering appears and of the blister characteristics. Similar results have been reported [5,6] although little attention was paid to the effect of the blistering on the silicon surface. In [4] we showed that, in the case of Aluminum capped Al_2O_3, not only blistering was observed but also silicon voids were detected after chemical etching of Al and Al_2O_3. In the present work, we study the effect of a post-deposition thermal treatment on the blistering of Al_2O_3 layers of different thickness and its effect on the silicon surface in Al-Al_2O_3-Si structures.

3. Experimental

The starting material used in this work is p-type Czochralski (100) silicon, with resistivity in the range of 0.1-1.4 Ω·cm. Al-Al_2O_3-Si capacitors were fabricated using a field isolated process, forming square active areas. Before Al_2O_3 processing, the wafers were cleaned in a H_2SO_4+H_2O_2 solution followed by a HF(5%) dip; therefore, all the deposition processes were performed on a hydrogen-terminated silicon surface. The studied Al_2O_3 layers were grown in a Cambridge NanoTech Savannah 200 system, using Trimethylaluminium and H_2O as precursors, and N_2 as carrier and purge gas. Al_2O_3 layers grown by means of 100 and 400 ALD cycles, leading to a thickness of 11 nm and 45 nm, respectively, were analyzed. After deposition an annealing step at 650ºC in N_2 for 30 min was done. Next, a 500 nm-thick Al/0.5%Cu layer was deposited and patterned to define the metal gate of the Al-Al_2O_3-Si structure. Finally, the wafers underwent a post-metallization annealing in forming gas (N_2/(10%)H_2) at 350ºC for 20 min.

After fabrication, optical inspection was used to assess the distribution and characteristics of the blisters. In order to evaluate the condition of the silicon surface, the Al and Al_2O_3 layers were etched off by means of a commercially prepared defreckling aluminum etch (DAE) acid. SEM imaging together with EDX analysis were used to analyze the revealed surface.

3. Results and discussion

Optical inspection of the fabricated samples confirmed that blistering is only observed in the areas corresponding to Al-Al_2O_3-Si, i.e., no blistering occurs when Al_2O_3 is deposited on the SiO_2 field oxide, indicating that blistering is related to adhesion of Al_2O_3 on Si. In addition, as shown in Fig.1, the dimensions and distribution of blisters are not uniform, even for structures of the same area.

After etching off the Al and Al_2O_3 layers, round silicon voids were observed on the silicon surface. The exact correspondence between the blisters and the silicon voids has been verified by SEM with the aid of fiducial marks done by FIB (Fig.2). A close analysis of the silicon voids shows that the round edge is extremely vertical and well-defined (Fig.3), which is an indication of the chemical nature of the effect rather than a consequence of mechanical stress. Since these silicon voids are only observed when the Al_2O_3 layer is capped with Al, this can be an indication of some chemical reaction at the Si surface underneath the blister. In all cases, EDX spectra indicated that only silicon is present in the surface of the samples after etching.

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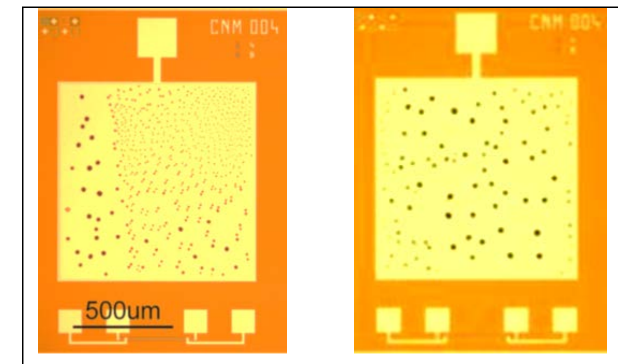

Fig.1. Optical image of the distribution of blisters in two 980x980 μm^2 Al-Al_2O_3-Si structures of the same wafer, for 45 nm-thick Al_2O_3.

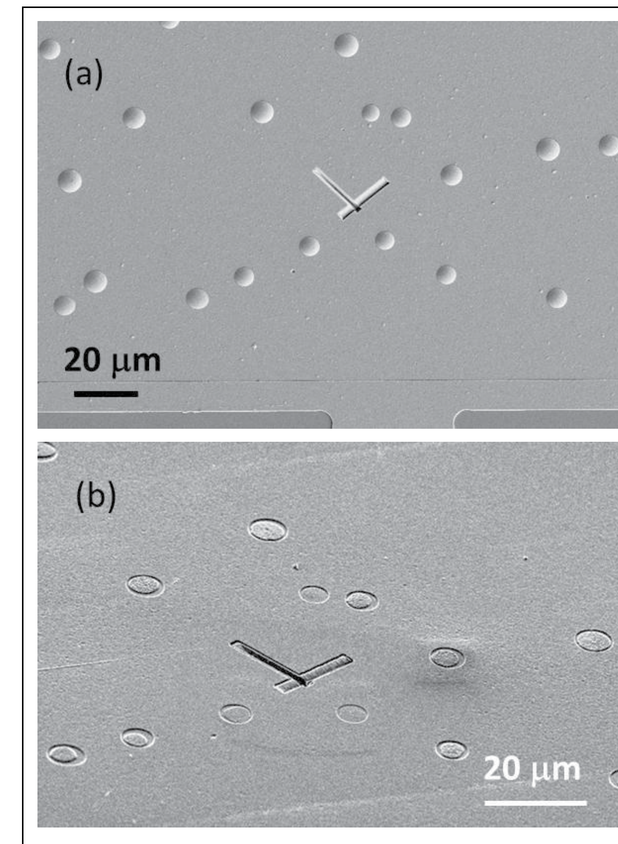

Fig.2. SEM image of (a) the aluminum surface showing the blisters and (b) the silicon surface after etching the Al and Al_2O_3 layers, corresponding to the 45 nm-thick Al_2O_3. The crossed bars patterns were done by FIB etching as a fiducial.

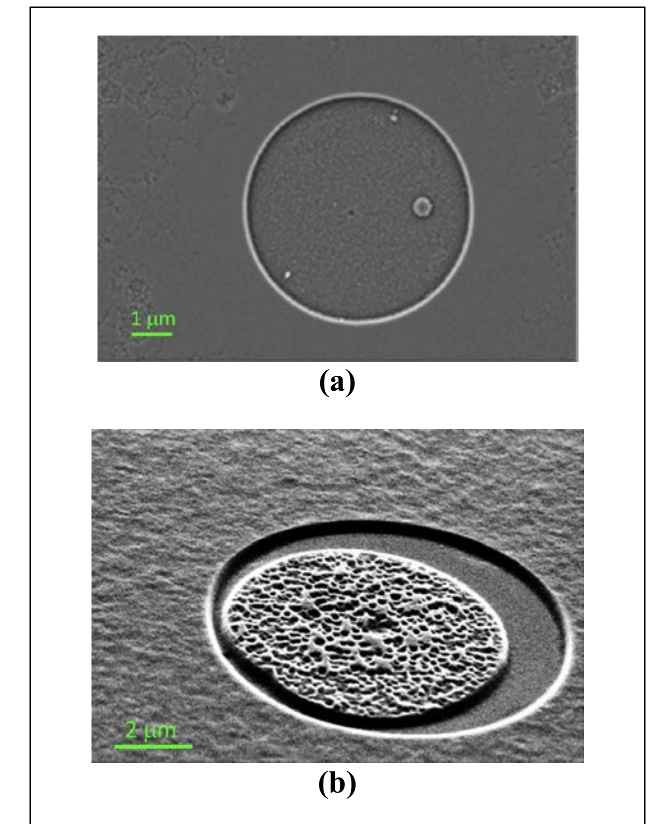

Fig.3. SEM images of the silicon voids revealed on the silicon surface after etching the Al and Al_2O_3 layers in structures with 11 nm-thick Al_2O_3 (a), and with 45 nm-thick Al_2O_3 (b).

Graphene transferred on atomic force microscope tips provides superior performance

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1. Introduction

Conductive atomic force microscope (CAFM) is one of the most powerful tools to characterize the electrical properties of a wide range of materials at the nanoscale. [1]. The main challenge associated to this technique is to ensure the reliability of the conductive tips. Traditional metal-varnished tips can wear out easily when measuring large currents or when exposed to high frictions. Poor tip reliability can not only result in false imaging, but it also increases the cost of the research. Therefore, finding a new method to avoid fast tip wearing is essential for cheap and reliable CAFM characterization. In this work, we show how to fabricate durable CAFM tips using a graphene coating, and compare endurance tests of standard and graphene-coated tips.

2. Experiment

Graphene single layer (GSL) sheets were grown on copper foils by Chemical Vapour Deposition (CVD) [2] and directly transferred onto Pt-Ir varnished CAFM tips. The process to coat the tip with graphene consisted of three steps: first, we immobilized the tip on a piece of silicon wafer using a thin film of Poly-methyl methacrylate (PMMA) below and on it; then this prepared block was used as the target substrate, and a graphene sheet was transferred on it (using PMMA as transfer media); finally, the PMMA layers were removed. The attachment of the graphene sheet to the tip was analyzed using the optical microscope, scanning electron microscope (SEM) and energy dispersive X-ray spectroscopy (EDX), and the lifetime of the tips was characterized in the CAFM using a GSL/Cu foil.

3. Results and discussion

Figure 1a shows the optical image of as-grown GSL on Cu. The typical copper steps and the copper grain boundaries can be observed, as previously reported. [2] Figure 1b shows the CAFM tip anchored to a silicon substrate and covered with the PMMA/GSL stack. After the Cu removal, the shape of the graphene on the Cu grain boundaries (arrows) can still be observed in the PMMA/GSL stack, indicating the presence of graphene on the tip. The cantilever slightly bends due to the weight of the PMMA. After soaking the tip in acetone, the PMMA was removed, the tip flexes back to its initial position and the graphene gets attached to the tip apex.

After the fabrication process, we prove the presence of graphene in different ways. Some areas of the tip show the presence of suspended graphene next to the cantilever edge (white arrows in Figures 1c and 2a). Moreover, SEM images taken on the GSL-coated tip show typical graphene domains (green arrow in Figure 2a). [3] Finally, EDX measurements reveal higher density of Carbon on the tip apex. Figure 2b shows the typical SEM image of the apex of a graphene-coated tip, and Figure 2c shows typical carbon signal collected with EDX. The higher density of carbon on the tip apex demonstrates that, despite the graphene could not cover the rough morphology of the whole chip, the graphene could successfully attach to the tip apex.

The lifetime of both standard and graphene-coated tips has been characterized by measuring sequences of current maps on a GSL/Cu stack until the tips lose their conductivity. Figure 3a shows the typical topographic AFM picture of the sample, and the copper steps can be clearly observed. Figures 3b and 3c show the last current maps collected with an as-received and a graphene-coated tip, respectively. Comparing the images it can be observed that as-received tips allow scanning an area of 90 μm^2 before losing the conductivity, while the graphene-coated tips show no current decay after scanning an area of 800 μm^2. The explanation for this observation is that the graphene layer effectively protects the metallic tip varnish from large current densities and frictions with the substrate, enhancing its lifetime.

4. Conclusion

In conclusion, we successfully fabricated durable CAFM tips, by coating commercially available metal varnished tips with a sheet of GSL, following the standard transfer process. The genuine properties of graphene can protect the tips from high currents and frictions with the sample, leading to much longer lifetimes, which remarkably reduces the cost of the research.

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Fig.1. Optical images of the (a) fresh GSL on copper, (b) PMMA/GSL stack transferred on the tip, and (c) graphene-coated tip after PMMA removal. The cantilever of the tip tends to bend due to the weight of the PMMA (b), and it recovers its initial position after removing it (c). The scale bars for (a), (b) and (c) are 200 μm, 500 μm and 200 μm, respectively.

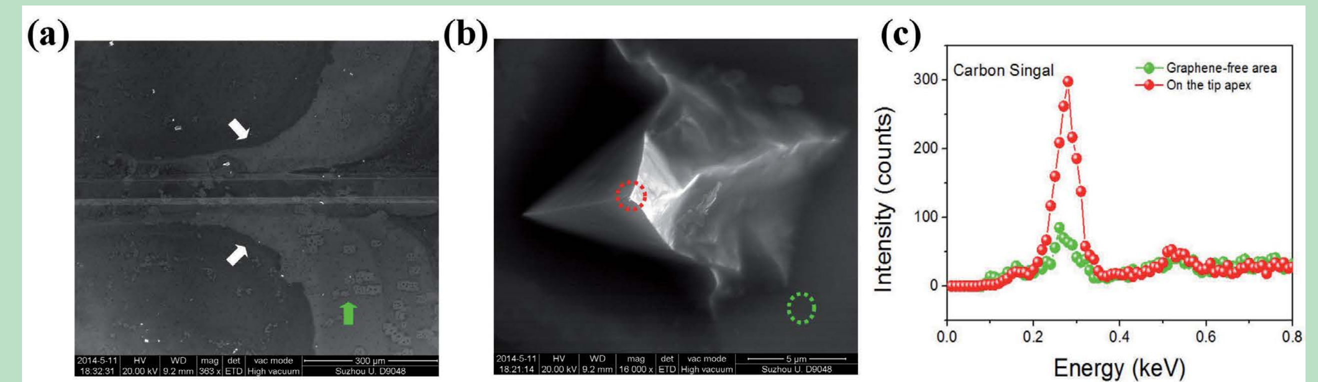

Fig.2. SEM images of (a) a cantilever covered with graphene, (b) the apex of a graphene-coated tip and (c) typical carbon signal collected with EDX. The white arrows in (a) point a part of suspended graphene on the cantilever, due to the rough morphology of the tip chip. The green arrow point the typical graphene domains related to graphene. The scale bars in (a) and (b) are 300um and 5um, respectively. The higher carbon signal on the tip apex (red circle in panel b) also demonstrates that the graphene attaches to the tip successfully.

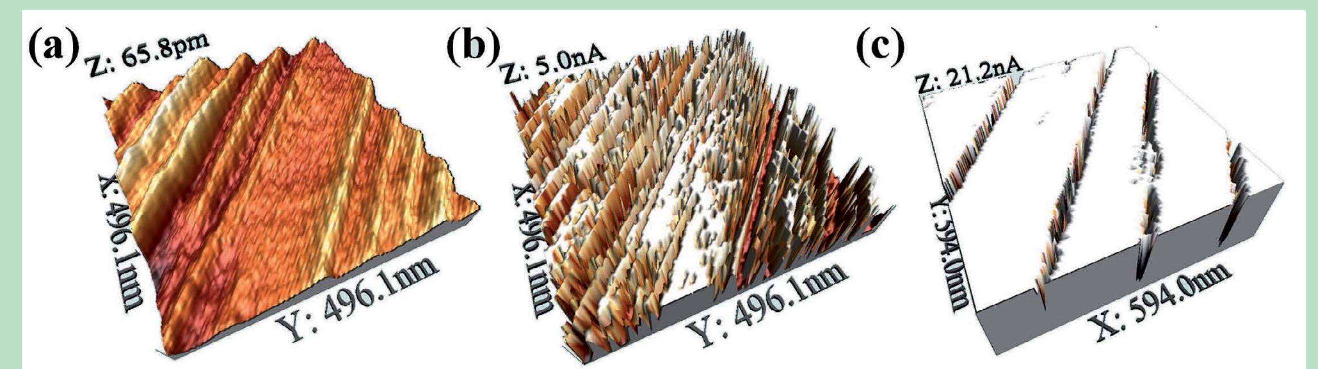

Fig.3. (a) 3D topographic map of a GSL/Cu stack. Last current map of a sequence of scans measured on a GSL/Cu stack using (b) a standard tip and (c) a graphene-coated tip. The total areas measured before figures (b) and (c) are 90 μm^2 and 800 μm^2. The lifetime of the standard tip is clearly enhanced thanks to the graphene coating, and larger currents can be measured even after using the tip to scan areas 10 times larger.

Synthesis and characterization of SnO_2 nanowires grown by CVD for application as gas sensors

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1. Abstract

Nanowires (NW) of tin oxide have been synthesized by chemical vapor deposition method (CVD) using Au as catalyst. The nanostructures were characterized with different analysis techniques (SEM, XRD and XPS) to study the effect of preparation conditions in the nanowire growth.The growth mechanisms of the nanowires were also discussed. NWs sensitive layers were tested as resistive sensors to acetone detection.

2. Introduction

Through last years, there has been an enormous interest in the research and development of semiconducting nanostructures due to their potential application in electronic devices as well as in the sensor field. Chemical sensors based on semiconductor nanostructures are expected to have a significantly enhanced performance than thin films due to the high surface-volume ratio. They are expected to be more stable and sensitive. Obviously, it would improve the sensitivity and selectivity and it would reduce the response and recovery times [1-2]. So semiconducting oxides such as ZnO, GeO_2, In_2O_3, SnO_2, and Ga_2O_3, have been synthesized into wire-like and belt-like nanostructures to be tested as gas sensors [3-5].

In this paper,we have researched the influence of the preparation conditions on the growth of SnO_2 nanowires by CVD method. The aim is to obtain nanowires with suitable characteristicsas sensitive materials to pollutants and hazardous gases

3. Experimental

SnO_2 NWs were grown by CVD process in a horizontal vacuum quartz tube furnace (ATOMATE- LPCVD system model HTF 55437C). For synthesis, a small amount of Sn (purity, 99.99%- Aldrich) powders was put in an alumina boat. The substrates used, were pieces of Si-SiO_2 (size 1x1 cm^2) with gold colloidal particles (Ted Pella, Inc) as catalysts.The samples were grown for 30 minutes at three temperatures 700, 800 and 900°C.Other variables as time and tin amount have also been considered and evaluated.

4. Results and discussions

The SEM micrographs revealed the formation of different nanostructures (nanoparticles, nanowires and nanobelts)depending on the growth temperature. Nanowire networks have been obtained at 800 °C under an Ar flow with oxygen traces, the nanowires have longer than 30 µm and diameters of 30-400 nm (fig. 1a). The nanowire growth takes place as a multiple nucleation (Fig. 1b). Also it is observed the presence of branched nanowires (Fig. 1b).

The samples prepared without catalyst showed a granular morphology with several structures (wires, belts, rods etc.) of micro- and nanometer dimensions without preferential growth areas (Fig. 2).

The growth mechanisms were discussed and the results proved that the growth of nanowires was carried out by a vapor–liquid–solid (VLS) process, where the catalyst is the key to the nucleation and growth of nanowires. However the existence of other nanostructures and the peculiarities found in the growth of nanowires (multiple nucleation) make us think that other mechanisms could take place simultaneously.The formation of the branched nanowires can be attributed to a self-catalytic mechanism which must be competitive with the growth in length of the wires by VLS.

Gas sensing properties of SnO_2 NWs were also investigated and tested as gas sensor (Fig. 3).

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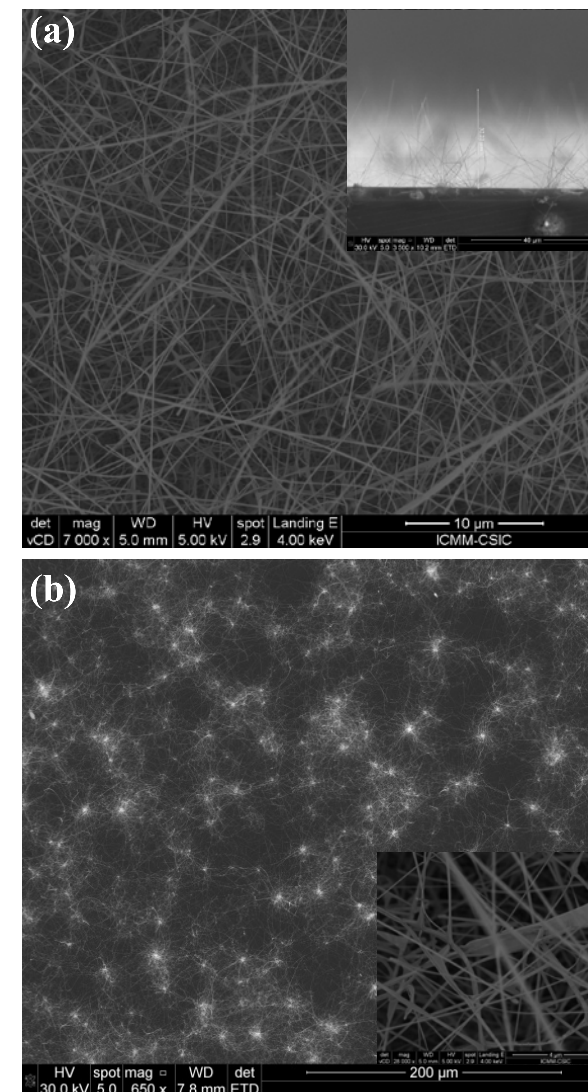

Fig. 1: SEM images of SnO_2 nanostructures grown at 800ºC on SiO_2-Si substrates with Au nanoparticle. (a) Detail of a cross-sectional view of nanowires grown perpendicular to the substrate. b) Detail of branched nanowires.

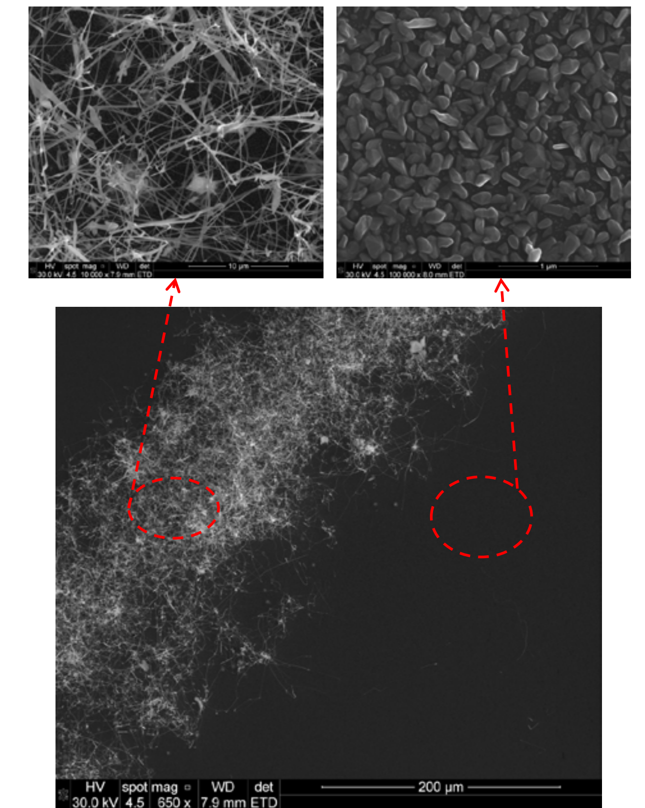

Fig. 2: SEM images of different morphologies of a sample grown at 800 °C without catalystand magnification of the area marked by circles.

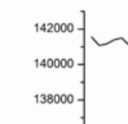

Fig. 3: Dynamic response of the SnO_2 nanowires to acetone at 350ºC.

Floating-Body-Correlated Subthreshold Behavior of SOI NMOS Device Considering Back-Gate-Bias Effect

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1. Abstract

This paper reports the floating-body-correlated subthreshold behavior of the SOI NMOS device considering the back-gate-bias effect. As verified by the experimentally measured data, when the channel length shrinks from 1μm to 120nm, the subthreshold slope becomes steeper due to the dominance of the parasitic BJT in the thin film. For the channel length becomes smaller further to 60nm, the subthreshold slope becomes less steep as a result of the dominating DIBL effect in the MOS channel region. As the device is biased at the back gate bias of 10V, for a long channel, the subthreshold slope is improved due to the enhanced function of the parasitic BJT and for a short channel of 60nm, the subthreshold slope is not improved due to the dominance of DIBL.

2. Introduction

PD SOI NMOS devices suffer from floating body effect, whose strong-inversion regime behavior has been studied [1][2]. The parasitic BJT in thin film plays an important role in the floating body effect [2]. In fact, the floating body effect may also affect the device behavior in the subthreshold regime. Furthermore, the characteristics of a PD SOI device may be further complicated by the back-gate-bias effect. In this paper, the floating-body-correlated subthreshold behavior of a PD NMOS device considering the back-gate-bias effect is described.

Fig. 1 shows the cross section of the PD SOI NMOS device under study. It has a gate oxide of 2nm and a thin film of 70nm doped with the p-type density of $2\times10^{18}cm^{-3}$[2]. Experimental measurement of the test device and 2D device simulation using a TCAD program have been done for the study.

3. Subthreshold Behavior

Fig. 2 shows the subthreshold characteristics of the PD SOI NMOS device with a channel length of 1μm, 0.5μm, 120nm and 60nm, biased at V_D=0.6V, 1.1V;V_B=0V, 10V. Fig. 3 shows the subthreshold S-factor versus channel length of the PD SOI NMOS device biased at V_D=0.6V, 1.1V ; V_B=0V, 10V and I_D=0.1 μA. As shown in the figure, when the channel length is scaled down from 1 μm to 120nm, the S-factor becomes better due to the dominance of the parasitic BJT in the thin film. A smaller channel length makes a stronger parasitic BJT, therefore a steeper subthreshold slope. When the channel length is shrunk further to 60nm, DIBL dominates the current conduction in the subthreshold regime. In addition, at the back gate bias of 10V, in the long channel regime, the parasitic BJT becomes stronger, hence the S-factor becomes better. In the short channel regime at 60nm, the back gate bias of 10V does not improve the S-factor since DIBL dominates. Fig. 4 shows the extracted I_C/I_D ratio and subthreshold S-factor of I_C versus channel length of the 60nm PD SOI NMOS device biased at V_D=0.6V, 1.1V; V_B=0V, 10V. As shown in the figure, in the long channel regime, the collector current (I_C)of the parasitic BJT dominates the drain current (I_D). In the short channel regime, DIBL in the MOS channel dominates. At the back gate bias of 10V, the parasitic BJT is even more important since the bottom MOS channel also turns on to trigger the parasitic BJT. In the short channel regime, the role of the back gate bias is not so substantially influential due to the DIBL dominance. Fig. 5 shows the 2D hole contours in the PD SOI NMOS device of channel length of 120nm, 60nm, and biased at V_B=0V, 10V, in the subthreshold regime at I_D=0.1μA. As shown in the figure, the trend on the 2D hole contours, which implies the strength of the parasitic BJT, for the cases with the channel length of 120nm, 60nm and V_B=0V, 10V correlates well to the behavior as indicated in Figs. 2-4.

4. Conclusion

In this paper, the subthreshold behaviour of the SOI NMOS device considering the floating body and back-gate-bias effects has been described. As verified by the measured data, when the channel length is scaled down from 1μm to 120nm, the subthreshold slope is steeper due to the dominance of the parasitic BJT. For the channel length becomes smaller further to 60nm, the subthreshold becomes less steep owing to the dominance of DIBL effect. As the device is biased at the back gate bias of 10V, for a long channel, the subthreshold slope is improved due to the enhanced function of the parasitic BJT and for a short channel of 60nm, the subthreshold slope is not improved due to the dominance of DIBL.

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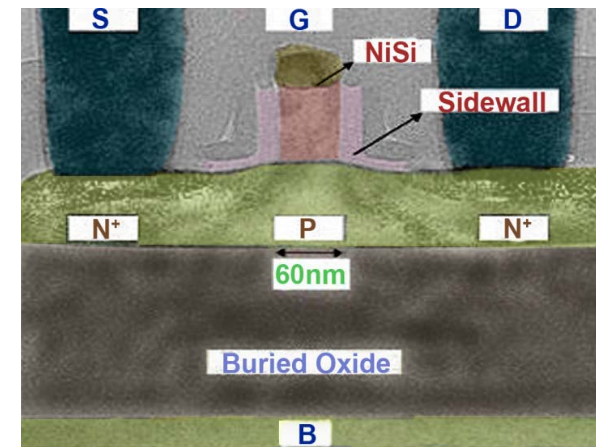
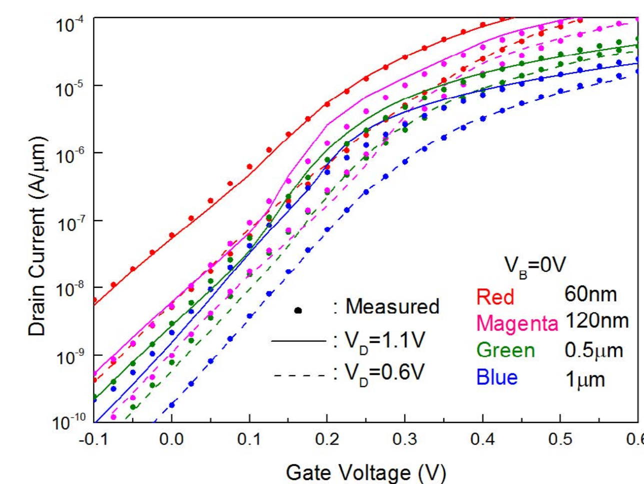


Fig.1. Cross section of the PD SOI NMOS device under study.



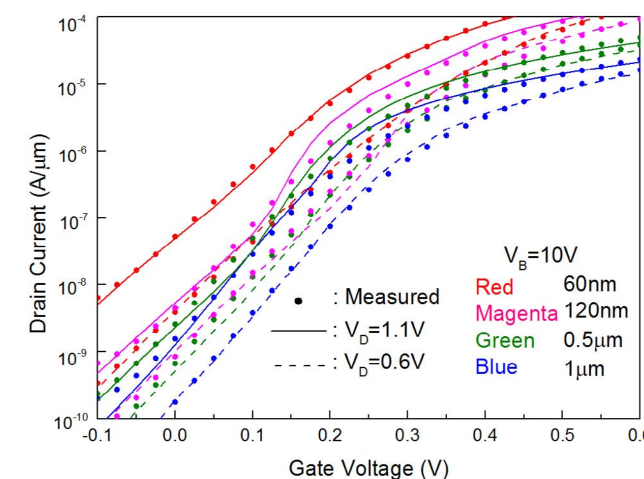


Fig. 2 I_D versus V_G of the 60nm PD SOI NMOS device of various channel lengths biased at V_D=0.6V, 1.1V; V_B=0V, 10V.

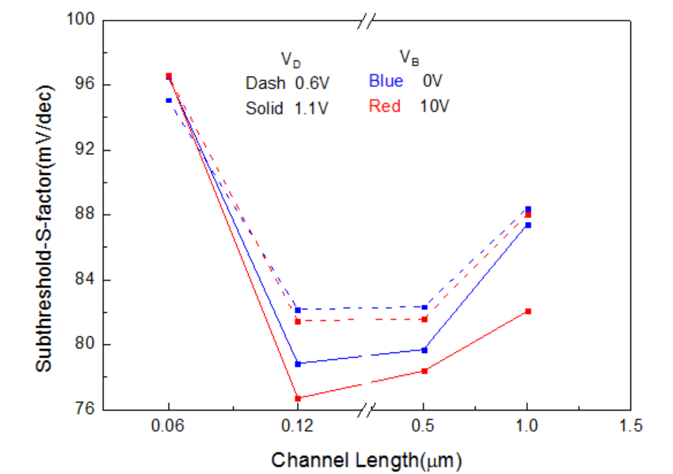


Fig.3. Subthreshold S-factor versus channel length of the PD SOI NMOS device biased at V_D=0.6V, 1.1V; V_B=0V, 10V and I_D=0.1 μA.

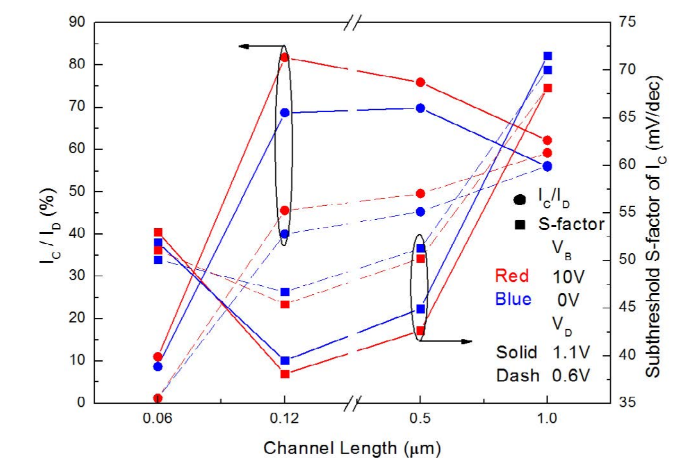


Fig. 4 The extracted I_C/I_D and subthreshold S-factor of IC versus channel length of the 60nm PD SOI NMOS device biased at V_D=0.6V, 1.1V; V_B=0V, 10V, I_D=0.1 μA.

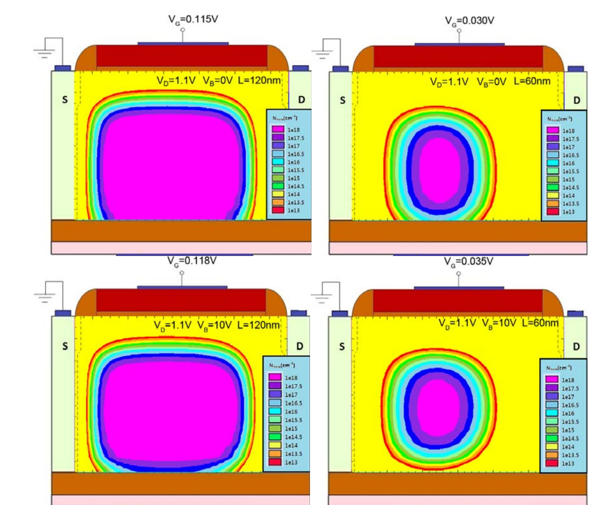


Fig. 5 2D hole contours in thin film of the PD SOI NMOS device of channel length of 120nm, 60nm, and biased at V_B=0V, 10V, in the subthreshold regime at I_D=0.1 μA.

Monte Carlo Modeling of Mobility and Microscopic Charge Transport in Supported Graphene

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1. Abstract

After the experimental demonstration of graphene [1], this exciting 2D material has received a huge amount of attention due to its electrical properties, which outperform those of conventional semiconductors: e.g., giant intrinsic mobility has been reported in suspended monolayer samples by both experiments and simulations [2], [3]. Nevertheless, graphene samples on an insulating substrate (which is unavoidable for most practical purposes) can present degraded electrical characteristics mainly due to the influence of substrate polar phonons [4]. Consequently, analyzing the influence of the underlying substrate on the electronic transport in graphene becomes a critical issue.

In this work, the influence of the underlying substrate and the temperature on relevant transport parameters such as the mobility, carrier energy or scattering time is analyzed by means of an ensemble Monte Carlo (EMC) simulator [5], [6]. Other phenomena of interest such as the origin of the negative differential conductivity behavior are also investigated. The graphene layer is considered to be a perfect 2D honeycomb, with no rippling, wrinkling, or impurities. The scattering mechanisms considered include intravalley and intervalley acoustic scattering, scattering with intrinsic optical phonons and surface polar phonon (remote phonon) scattering, or SPP. The SPP scattering rate is incorporated taking into account the formulation from previous works by other authors [4], [7], paying particular attention to the Coulombic, anisotropic nature of this kind of interaction (Fig. 1). In particular, the angle dependence of the scattering probability integrand (including the angular dependence of the Thomas-Fermi parameter) is considered. The SPP phonon energies considered are detailed in [6].

Mobility calculations are carried out in two separate ways. At low fields, it can be directly obtained from the velocity-field curves, which present a linear dependence in this regime. Both at low and high fields the mobility can be also obtained from the diffusion coefficient (provided by the second central moment in the EMC simulation) through the Einstein relation applied to the graphene case. A good agreement is obtained at low fields between both calculations.

The low-field mobility is significantly affected by the temperature considered and the substrate type (Fig. 2). At low temperature (50K) the maximum mobility reaches $2.8 \cdot 10^6$ cm^2/Vs, with no significant differences between suspended samples and graphene on h-BN and SiC, with SiO_2 and particularly HfO_2 yielding much smaller values. At room temperature, suspended graphene gives the largest low-field mobility value (500,000 cm^2/Vs), followed by h-BN (270,000 cm^2/Vs), SiC (220,000 cm^2/Vs), SiO_2 (98,000 cm^2/Vs) and HfO_2 (7,100 cm^2/Vs).

The influence on electron transport of the substrate type and the effect of SPP anisotropy on the negative differential conductivity is exhaustively analyzed. As an example we present here the results for average energy (Fig. 3), parallel wavevector (Fig. 4) and average time between scatterings (Fig. 5) as a function of the applied electric field, which will be discussed in the paper.

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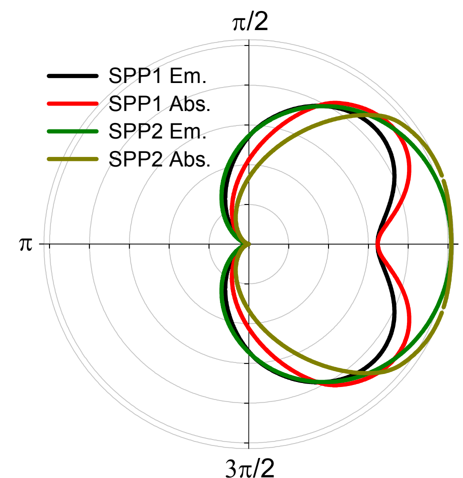

Fig.1. Angular distribution of the SPP emission and absorption probability in the case of SiO_2 substrate and energy equal to 0.25 eV. SPP1: low energy phonon. SPP2: high energy phonon.

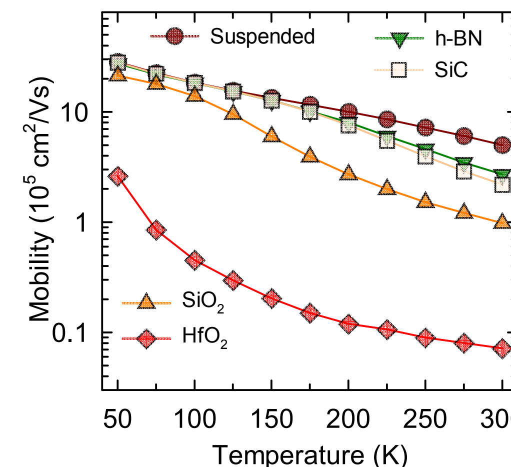

Fig.2. Low-field mobility as a function of the temperature for suspended graphene, graphene on h-BN, SiC, SiO_2 and HfO_2.

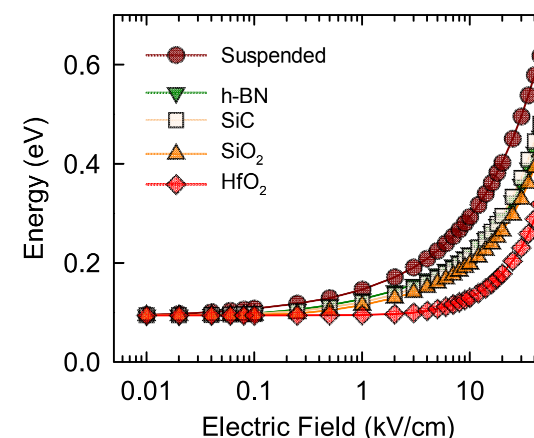

Fig.3. Average carrier energy as a function of the applied electric field for suspended graphene, graphene on h-BN, SiC, SiO_2 and HfO_2.

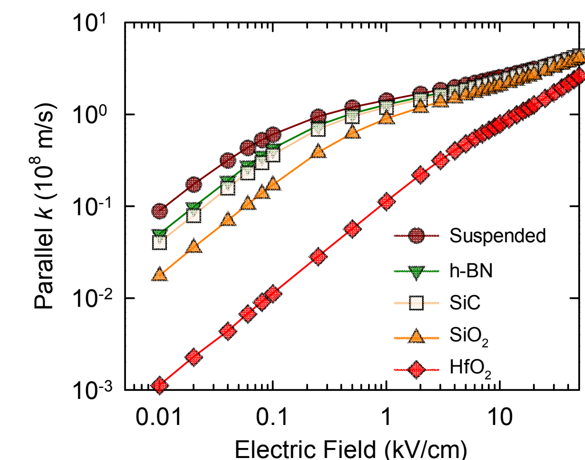

Fig.4. Average parallel wavevector as a function of the applied electric field for suspended graphene, graphene on h-BN, SiC, SiO_2 and HfO_2.

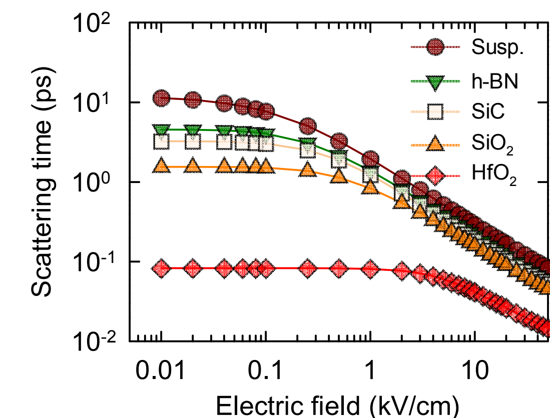

Fig.5. Average scattering time as a function of the applied electric field for suspended graphene, graphene on h-BN, SiC, SiO_2 and HfO_2.

Raytracing and electromagnetic 2-D simulations of the EQE of a-Si:H thin-film solar cells

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Thin-film amorphous silicon (a-Si:H) solar cells have become of great interest due to their reduced price. However, they depend on light confinement to improve their efficiency. These so-called light trapping techniques include texturized front contacts to scatter the light, and reflective rear contacts to promote the absorption at long wavelengths (λ) [1,2]. The dual nature of light compels the use of advanced simulation tools to model these optic phenomena [3].

In the present research work we compare the results obtained considering first light as a particle and subsequently, simulating it as a wave. For the first case we used Monte Carlo ray tracing (RT), and for the second one an electromagnetic wave finite-difference time-domain software (FDTD). Both tools are available in Sentaurus TCAD suite (Synopsys) [4].

The electric parameters necessary to fit the dark and illumination I-V curves were presented in previous works [5]. The characteristic that we reproduced in the present paper is the external quantum efficiency (EQE) in the stabilized state of the cell (after 300 hours of illumination). This trait describes the efficiency of the photon-to-electron conversion for each λ.

The device under analysis is a 1cm^2 cell. It is made up of a glass substrate with a transparent conductive oxide (TCO) as front contact. This had a random texture with an average root mean square height of 43.19 nm and around 230 peaks every 25 µm^2.

The a-Si:H layers were deposited over the glass via plasma enhanced chemical vapor deposition (PECVD); first, a 10 nm p-layer (doped with boron), next a 200 nm (± 0.8%) i-layer (intrinsic) and finally a 10 nm n-layer (doped with phosphorus). The back contact consists of a transparent aluminum zinc oxide (AZO) layer, and a reflective aluminum layer.

Figure 1 shows a scheme of the simulated structure using RT. The texture in the TCO/p-layer interface consists of triangles with a height of 20 nm and a base of 200 nm. This was optimized in past works [6]. RT calculates the transmitted, reflected and absorbed components of light; building a tree for each one of the 5000 input rays.

The FDTD software solves thoroughly the Maxwell equations. Since a discretization in the time and space domains is performed, this type of simulation has a high computational cost. Therefore, we made a simplification of the structure, using only two points of texture (see figure 2). Additionally, periodic boundary conditions were assumed, and the i-layer thickness was varied to reproduce its slight non-uniformity.

In figure 3 we show the comparison of the experimental EQE (measured with a traditional spectral response system) and the simulated ones. Despite the fact that the efficiency at short λ is overestimated and slightly underestimated in the 400-530 nm range, the fitting is overall good with the two methods. Nonetheless, the effects of the interference around 600 nm can only be seen with the FDTD tool, RT is unable to reproduce them.

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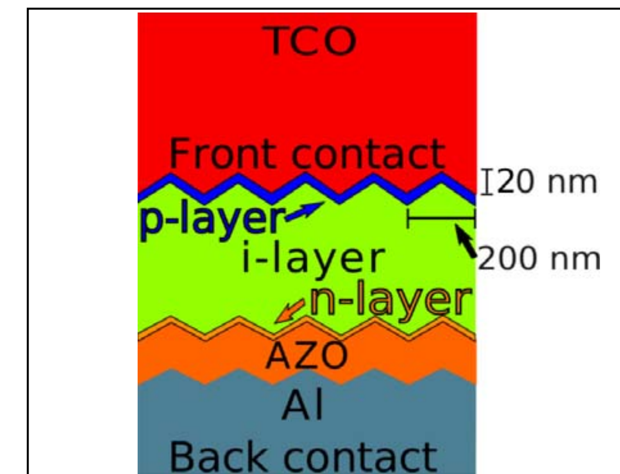

Fig.1. Scheme of the structure employed in the RT simulation. The texture in the TCO/p-layer interface consists of triangles with a height of 20 nm and a base of 200 nm. The height is diminished in the subsequent layers assuming this is what happens as layers are deposited.

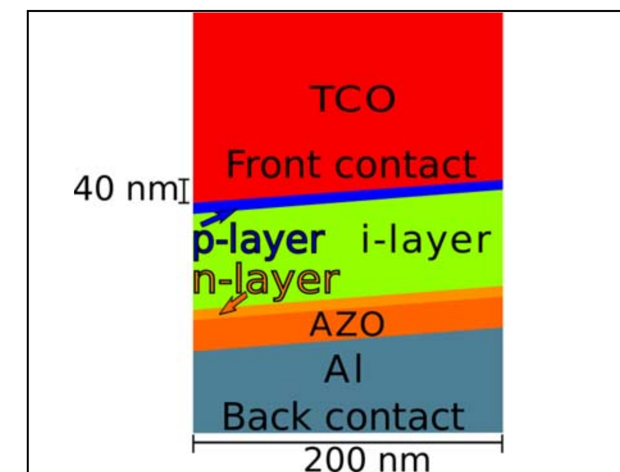

Fig.2. Scheme of the structure employed in the FDTD simulation. To diminish the simulation time the texture in the TCO/p-layer interface was simplified using only two points (a height of 40 nm and a base 200 nm). The height is decreased in the following layers. The thickness of the i-layer was varied to reproduce the effect of its slight non-uniformity.

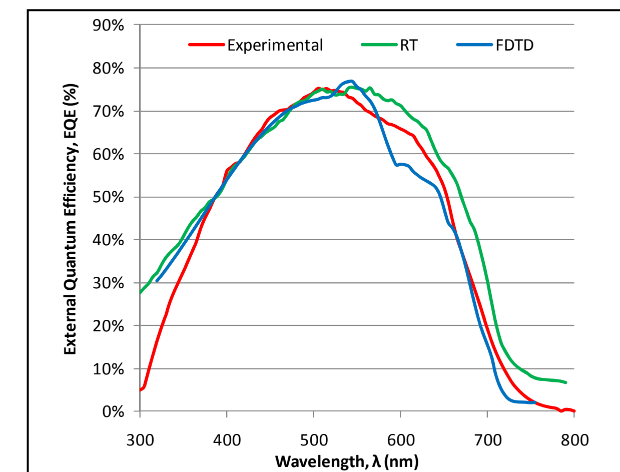

Fig.3. Results of the RT and FDTD simulations compared with the experimental EQE. The red curve represents the experimental EQE while the green and blue ones correspond to the RT and FDTD simulations, respectively.

Effect of nanofluid conductivity and humidity on the self-assembly of colloidal crystals by means of electrospray

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1. Abstract

Nowadays nanostructures are gaining importance in several fields due to its high surface area ratio and its optical and electrical properties. The two main approaches for the formation of nanostructures are top-down or bottom-up. Top-down techniques usually require expensive equipment such as electron-beam lithography that is restricted to very small areas and henceforth to sequential processing. On the contrary, bottom-up strategies are able to produce several samples and structures simultaneously. Of course self-assembly of nanoparticles or nanocomponents is mostly welcome as avoids many of the problems of the other conventional techniques. Today colloidal crystals are produced using many of both categories of technologies, but one of the main problems still unsolved is the small size of the areas of the samples (typically few square millimeters) and ordering range of nanoparticles of few micrometers.

Photonic crystals are nanoparticle arrangements with random hexagonal close packed shape (RHCP) order. This 3D periodicity enhances light reflection at wavelength proportional to the size of the nanoparticles. We have recently shown that electrospray of nanofluids has the capability to induce the colloidal crystal formation [3-5] in big areas and with good optical quality and short processing time.

The complexity of the deposition technique requires to adjust fabrication parameters, such as the liquid pumping rate and the electrical conductivity. In our observations, we have identified as one of the key factors the presence of some liquid on the substrate while the nanoparticles are self-assembling.

In the present work we show results of these observations concluding that the value of the nanofluid conductivity has an important effect on the amount of liquid reaching the substrate and the time remaining there before evaporation. At the same time the liquid enables the ordering of nanoparticles. We have seen that several layers of ordered nanoparticles can be produced if the substrate is wet while the absence of water produces monolayers of scattered nanoparticles, but not large area order.

In our interpretation, the several forces that play a significant role in the deposition process, namely, drag force, buoyancy, weight and dielectrophoresis, combine among them to facilitate the self-assembly conditions. While the buoyancy and weight cancel each other in the dimensions of our work, and even if the drag force is very small, the change of the dielectric permittivity of the medium due to the humidity can be fundamental in the process.

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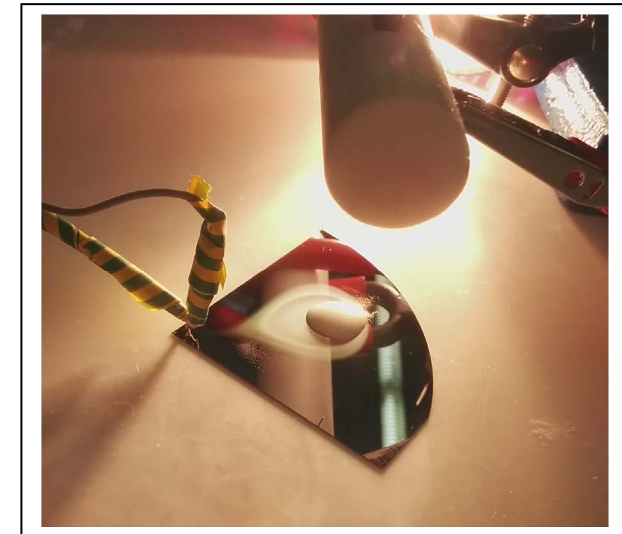

Fig.1. Electrospray setup with some nanofluid accumulated in the sample

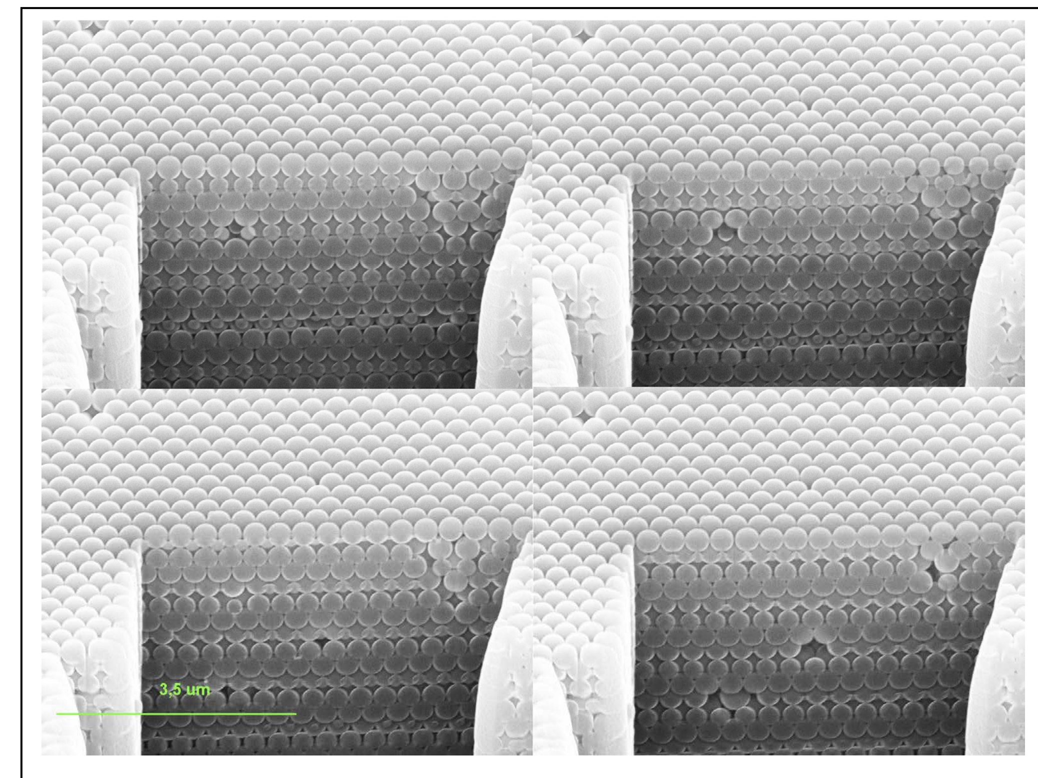

Fig.2. SEM images from the sample with 4 crosssections at 80nm distance

Electrical characterization of MIS capacitors based on Dy_2O_3-doped ZrO_2 dielectrics

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1. Introduction

High-k dielectric materials are critical for the *state of the a*rt integrated circuits. They should replace silicon dioxide as a gate dielectric in MOS transistors in order to reduce the off state leakage current due to direct tunneling [1]. Zirconia and hafnia are two of the most studied materials for this purpose. It is also known that rare earth oxide doping can stabilize high permittivity phases of hafnium and zirconium oxides [2,3].

In this work we studied the electrical properties of metal-insulator-semiconductor (MIS) structures using zirconium oxide (ZrO_2) doped with dysprosium oxide (Dy_2O_3) as the gate dielectric. The amount of dysprosium in the films was varied and the influence of the doping level and post-deposition annealing on the properties of the MIS capacitors was studied.

2. Experimental

Dielectric films were grown by atomic layer deposition (ALD) on p-type Si(100) substrates. $ZrCl_4$ and $Dy(thd)_3$ were used as metal precursors, and water was used as the oxygen precursor. Dy_2O_3 doped ZrO_2 films were grown as stacks of alternating layers of undoped and doped ZrO_2. The compositions and thicknesses of the films measured by ERDA and ellipsometry, respectively, are presented in Table 1. Some of the samples were annealed after ALD at 700 ºC for 30 minutes in oxygen atmosphere.

The MIS structures were prepared by evaporation of 0.204 mm^2 Ti/Al dots on ZrO_2 and ohmic Al on Si. The electrical properties were studied using capacitance-voltage (C-V) and current-voltage (I-V) measurements, deep level transient spectroscopy (DLTS) and characterization of flat-band voltage transients (Vfb-t).

3. Results

The ALD process used allowed deposition of films with relatively uniform thickness on planar as well as 3D substrates. The interface trap density measured by DLTS did not depend markedly on the amount of dysprosium present in the dielectric layers (Figure 1). This could be due to the fact that deposition of the dielectric was started with undoped ZrO_2 and the composition of the material that was in direct contact with the silicon substrates did not vary considerably in as grown samples. Annealing of the samples at 700 ºC caused increase in the interface state density regardless the amount of dysprosium in the films while again no significant effect of dysprosium content was found.

By contrast the hysteresis amplitude of capacitance-voltage characteristics measured for as-deposited capacitors decreased with increasing dysprosium concentration in the dielectric (Figure 2). This means the Dy doping reduced the slow trap density inside the ZrO_2 films. Surprisingly, annealing caused an increase in the trap density also inside the films.

Flat-band voltage transients were measured for the different samples. Figure 3(a) shows the flat-band voltage transients measured at different temperatures for and annealed capacitor based on the structure C521. Figure 3(b) shows the Arrhenius plot for the transients plotted in Figure 3(a) and the activation energy obtained in this case. These transients are related to the hysteresis obtained in C-V measurements: the bigger the hysteresis, the bigger the transient amplitude.

Finally, current-voltage characteristics were measured for the different capacitors. The addition of dysprosium to the zirconium oxide films reduced the leakage current density, possibly due to the reduction of the defect concentration inside the oxide, as it was concluded from the C-V curves.

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Table 1. Composition and film thickness

Sample No	Composition by ERDA, at%						Thickness by ellipsometry
	H	C	O	Cl	Zr	Dy	
C520	8.7	1.6	60.0	1.2	28.1	0.4	40.9nm
C521	12.0	1.6	56.9	1.9	26.3	1.3	44.0nm
C522	13.0	1.5	56.1	2.9	25.1	1.4	61.9nm

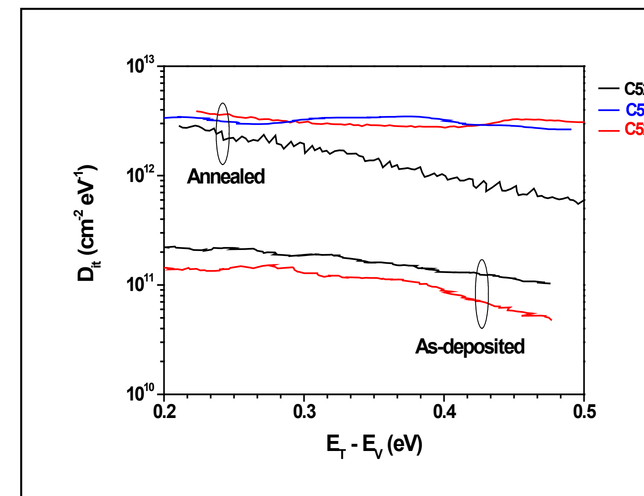

Fig.1. Interface state density measured by deep level transient spectroscopy

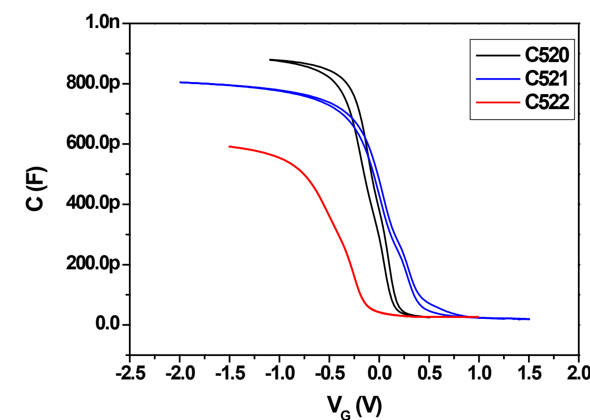

Fig.2. Capacitance-voltage curves for the as-deposited capacitors

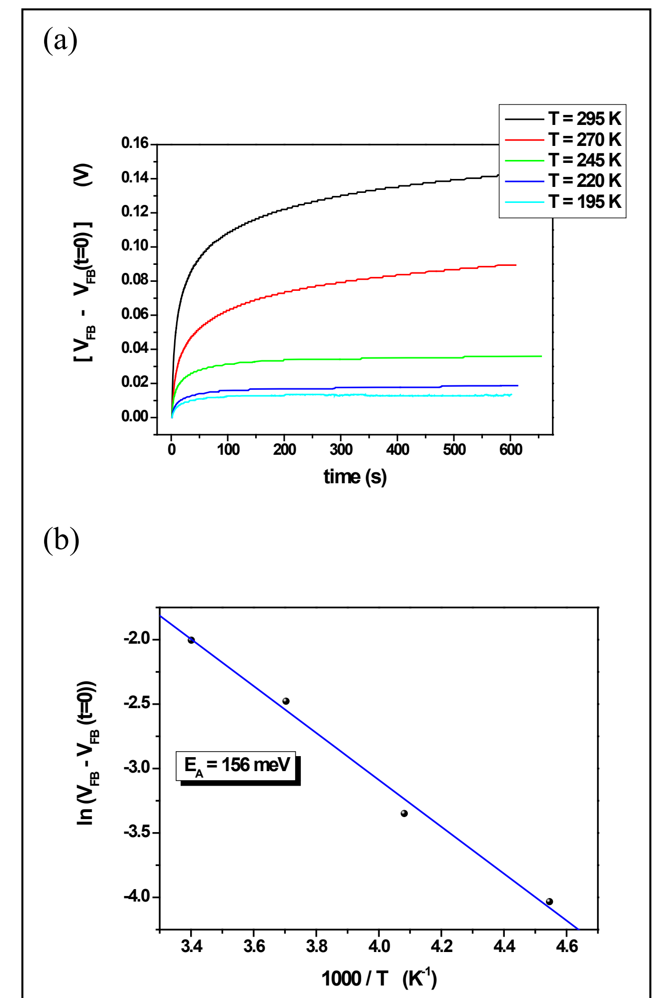

Fig.3. Flat-band voltage transients measured at different temperatures for the C521 Annealed sample (a) and Arrhenius plot obtained for the transients (b).

Deep level defects in *mono-like*, *quasi-mono* and multicrystalline silicon solar wafers

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1. Introduction

Nowadays in the photovoltaic (PV) industry nearly a 90 % of the world production is based on monocrystalline (sc-Si) and multicrystalline (mc-Si) silicon substrates. Specifically, mc-Si wafers constitute a profitable option to cover the silicon PV demand because of its low manufacturing cost despite its lower performance compared to sc-Si wafers. Thus, the PV market demands new types of wafers with monocrystalline features using common cast growth furnaces such as the *quasi-mono* (qm-Si) and *mono-like* (ml-Si) wafers [1].

However, the efficiency of the solar cells based on qm-Si and ml-Si wafers still suffers serious drawbacks, such as the presence of dislocations and sub-grain boundary defects. In particular, deep level defects have been reported [2] as responsible of the strongly degradation of the solar cell efficiency.

The present work reports some experimental results of the electrical and optical properties of these three types of substrates: qm-Si, ml-Si and mc-Si.

2. Experimental

Several samples from all three types of wafers were analyzed with different characterization techniques.

By means of the light beam induced current (LBIC) technique we determine the structural heterogeneities giving us an indication of the material quality and its suitability for solar cell use.

Thermal admittance spectroscopy (TAS) has been used for the characterization of the deep levels related to such heterogeneities and impurities in the silicon substrates. TAS is a technique which yields thermal emission rates (e^t_p) of deep levels from the variations of capacitance and conductance of the junction when the frequency of the measuring signal is fixed and the temperature is scanned. Each deep level existing in the junction yields a maximum in conductance (G_m) at a temperature T_m. The thermal emission rate is given by:

$$e^t_p(T_m) = \omega/1.98 \qquad (1)$$

where ω is the frequency of the measuring signal. If we repeat the measurement varying the frequency value we will obtain the thermal dependency of e^t_p, from which the activation energy (E_T) and the capture cross section (σ_T) can be derived according the Arrhenius law:

$$e^t_p(T) = \sigma_T \gamma T^2 \cdot \exp(-E_T/kT) \qquad (2)$$

3. Results

Figs.1 and **2** show the admittance spectra for a mc-Si sample and a ml-Si sample, respectively. In these curves we can see that conductance peak hardly depends on the frequency, so indicating that only one deep level, in first approximation, is present in the samples.

Using (1) we can obtain the values of e^t_p for each frequency in each sample. If now we plot $ln(e^t_p/T^2)$ vs. $1/kT$ for each sample, according to (2), the slope of the linear fit is E_T and from the origin ordinate we can obtain the σ_T value. **Figs.3** and **4** show these plots for the mc-Si and ml-Si samples, respectively. All results are summarized in **Table 1**.

4. Discussion and Conclusions

This work reveals two types of deep levels present in our samples both associated to Fe. On one hand we have the values between 325 and 373 meV present in mc-Si and mq-Si, with σ_T in the order of 10^{-13}-10^{-11} cm^2. The high σ_T value could be due to the segregation of Fe to the extended defects. On the other hand we have the values between 171 and 291 meV, with σ_T values in the order of the reported by other works for these punctual defects. This type is present in mc-Si samples for some bias values together with the first type. It is present alone in qm-Si samples for some bias values and in ml-Si samples for all bias values.

The differences in efficiency among ml-Si and mc-Si solar cells, about 0.25 % [3], could be due to the difference in the substrate quality. The reason why the efficiency difference is not very high is because the total amount of iron is very similar in all samples.

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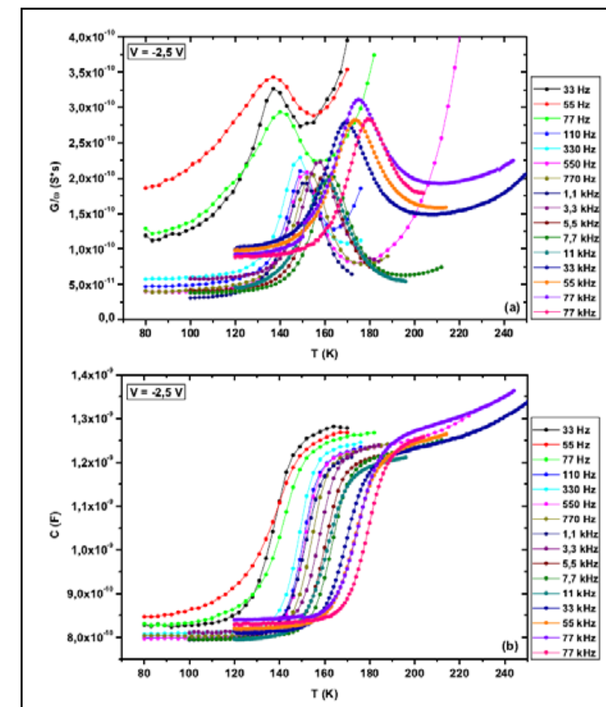

Fig.1. Admittance spectra for a mc-Si sample where (a) show the conductance vs. temperature curves and (b) show the capacitance vs. temperature curves.

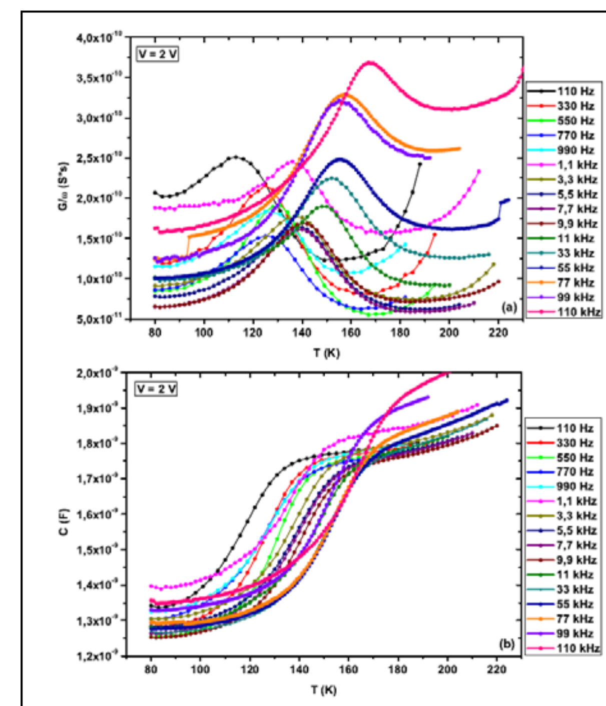

Fig.2. Admittance spectra for a ml-Si sample where (a) show the conductance vs. temperature curves and (b) show the capacitance vs. temperature curves.

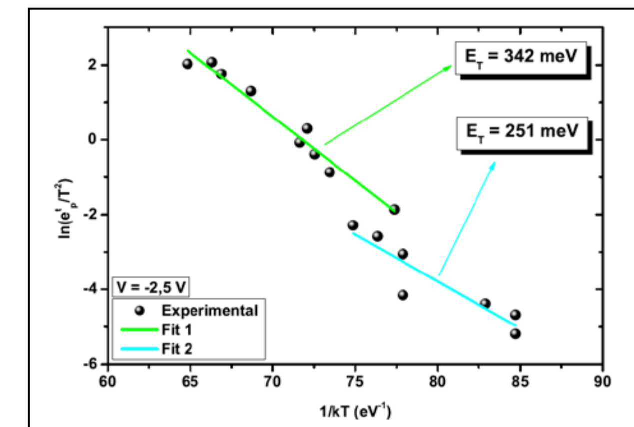

Fig.3. Arrhenius plot for a mc-Si sample

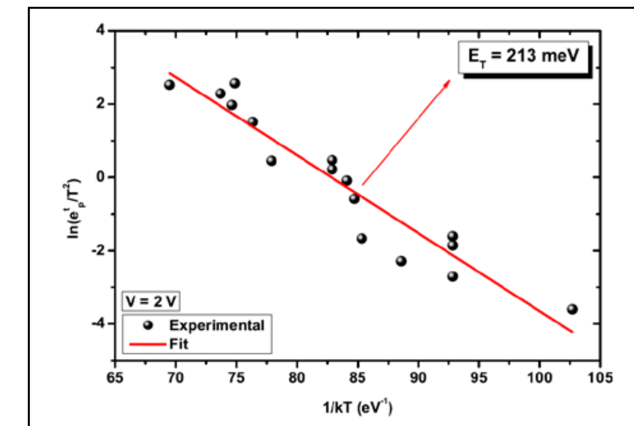

Fig.4. Arrhenius plot for a ml-Si sample

Type	Bias (V)	E_T (meV)	σ_T (cm^2)
mc-Si	-2.5	342 & 251	$2.54 \cdot 10^{-11}$ & $6.56 \cdot 10^{-15}$
	1.0	325	$1.62 \cdot 10^{-11}$
	1.5	336 & 171	$2.65 \cdot 10^{-13}$ & $3.98 \cdot 10^{-18}$
qm-Si	-2.0	373	$3.61 \cdot 10^{-12}$
	-1.0	291	$1.82 \cdot 10^{-14}$
	-0.5	271	$6.79 \cdot 10^{-16}$
ml-Si	0.5	218	$4.34 \cdot 10^{-15}$
	2.0	213	$2.55 \cdot 10^{-14}$
	3.0	224	$2.70 \cdot 10^{-14}$

Table 1. List of the analyzed samples. The substrate type (Type), the voltage used in the measurement (Bias), the obtained activation energies (E_T) and the capture cross section (σ_T) are listed.

The Meyer-Neldel Rule in the properties of the deep-level defects present in silicon supersaturated with titanium

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1. Introduction

In 1997 A. Luque and A. Martí [1] proposed that the formation of an intermediate band (IB) in the mid gap of a semiconductor could have potential for drastically improving the efficiency of single junction solar cells. This approach would enable electrons to be pumped from the valence band into conduction band via two-photon absorption of photons with lower energy than the semiconductor band gap [2]. So, single junction solar cells based on a semiconductor with an IB could reach efficiency values above the maximum theoretical efficiency for single junction cells: 40.7 % [1]. IB solar cells could reach an efficiency value up to 63.1 %.

Trying to obtain some evidence of the existence of the IB en Ti supersaturated silicon substrates using the thermal admittance spectroscopy (TAS) technique, we founded out a particular relationship among the activation energy (E_T) and the capture cross section (σ_T) of all levels detected in the silicon band gap of samples with Ti concentrations under the Mott limit. This relationship is called the Meyer-Neldel rule [3] and establishes that in magnitudes with Arrhenius dependence, like the emission rate of a deep level:

$$e^t(T) = \sigma_T v_{th} N_C \cdot e^{-E_T/kT} \qquad (1)$$

there is a dependence among the pre-exponential factor and the activation energy like this:

$$\sigma_T = \sigma_{TT} \cdot e^{E_T/kT_{mn}} \qquad (2)$$

where T_{mn} is called Meyer-Neldel temperature and kT_{mn} the Meyer-Neldel energy.

2. Experimental

300 μm Si (111) n-type samples (μ=1450 cm^2/Vs; n=2.2x10^{13} cm^{-3} at room temperature) were implanted at 32 KeV with Ti at high doses: 10^{13} (UM1) and 10^{14} (UM2) cm^{-2}, with Ti profiles below the Mott limit at any depth. Then, the samples were annealed by means of the pulsed laser melting (PLM) method to recover the crystal lattice with one 20 ns long pulse at energy density of 0.8 J/cm^2.

TAS is a technique which yields thermal emission rates of deep levels from the variations of capacitance and conductance of a p-n or Schottky junction as a function of temperature and frequency. These variations are due to the change in frequency of the measuring signal with respect to the time constant of charge and discharge processes of the deep levels. Measurements consist on recording the capacitance and conductance variation of a bipolar junction as a function of temperature at a given frequency. Each deep level existing in the semiconductor band gap contributes with a peak in the conductance signal related to the deep level emission rate by the well-known equation:

$$e^t(T_{peak}) = \frac{\omega}{1.98} \qquad (3)$$

where ω is the angular frequency. The energy location and the capture cross section of the deep level can be obtained from equation (1).

3. Results and discussion

Table 1 shows the E_T and σ_T values obtained in the two samples at different bias values. In both samples it is found a set of bias values in which TAS detects only one deep level lead by the Ti implantation. **Fig. 1** shows the G/ω-T characteristics and the Arrhenius plot for UM1 sample biased at 0 V, in which a single peak appears in each curve. For the remaining bias values a couple of peaks appear in each curve. **Fig. 2** shows these curves and the associated Arrhenius plot for UM2 sample biased at -1 V.

A thorough examination of Table 1 notices that there is a dependency among σ_T and E_T values of all deep levels detected. In fact, this dependence fits to a linear relationship (**Fig. 3**), as the Meyer-Neldel rule establishes. From this fit kT_{mn}=15 meV and T_{mn}=176 K values are obtained.

4. Conclusions

As it is known, the Meyer-Neldel rule takes place in disordered systems where processes affected by this rule involve multiple excitations [4]. The carrier emission/capture by a deep level is a process in this way. The implantation layer of the silicon supersaturated substrates could be a region high disordered. So, there is evidence of the Meyer-Neldel rule in the samples studied that affects to the distribution of the deep levels in their band gap.

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Sample	Bias (V)	E_T (meV)	σ_T (cm^2)
UM1	-7.5	454	$8.71\cdot10^{-8}$
	-5	307	$5.50\cdot10^{-12}$
	-4	290	$2.94\cdot10^{-12}$
	-3	233	$1.09\cdot10^{-13}$
		451	$2.23\cdot10^{-7}$
	-2	173	$2.39\cdot10^{-15}$
		460	$4.08\cdot10^{-7}$
	-1	88	$3.85\cdot10^{-18}$
		427	$1.65\cdot10^{-8}$
	0	391	$1.23\cdot10^{-9}$
UM2	-7.5	365	$2.88\cdot10^{-10}$
	-5	335	$6.91\cdot10^{-11}$
	-4	303	$8.46\cdot10^{-12}$
	-3	238	$1.11\cdot10^{-13}$
	-2	193	$8.13\cdot10^{-15}$
	-1.25	129	$1.19\cdot10^{-16}$
		277	$3.20\cdot10^{-12}$
	-1	86	$3.92\cdot10^{-18}$
		264	$7.70\cdot10^{-13}$
	-0.75	66	$1.44\cdot10^{-18}$
		274	$2.40\cdot10^{-12}$
	0	287	$3.07\cdot10^{-12}$

Table 1. List of the analyzed samples. The voltage used in the measurement (Bias), the obtained activation energies (E_T) and the capture cross section (σ_T) are listed.

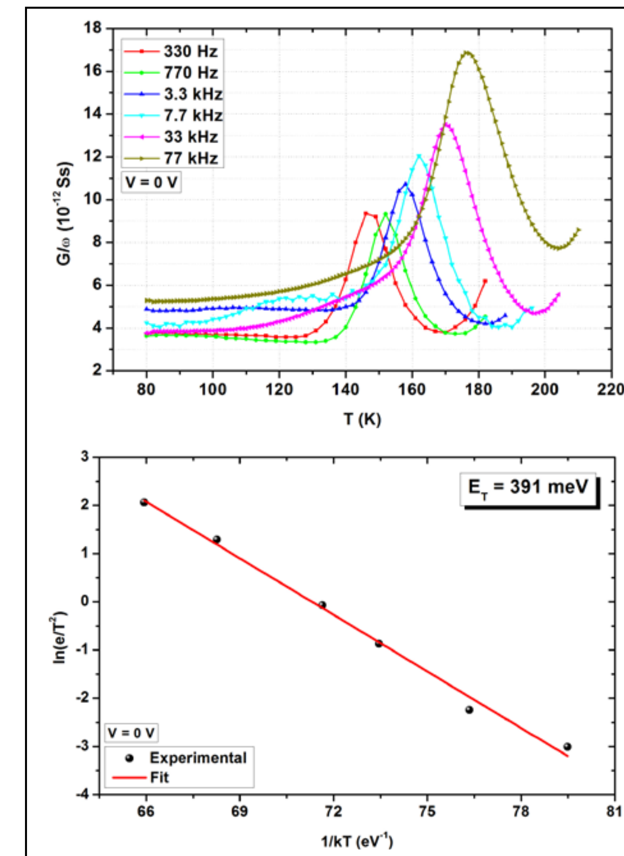

Fig.1. G/ω-T curves and Arrhenius plot for the UM1 sample biased at 0 V.

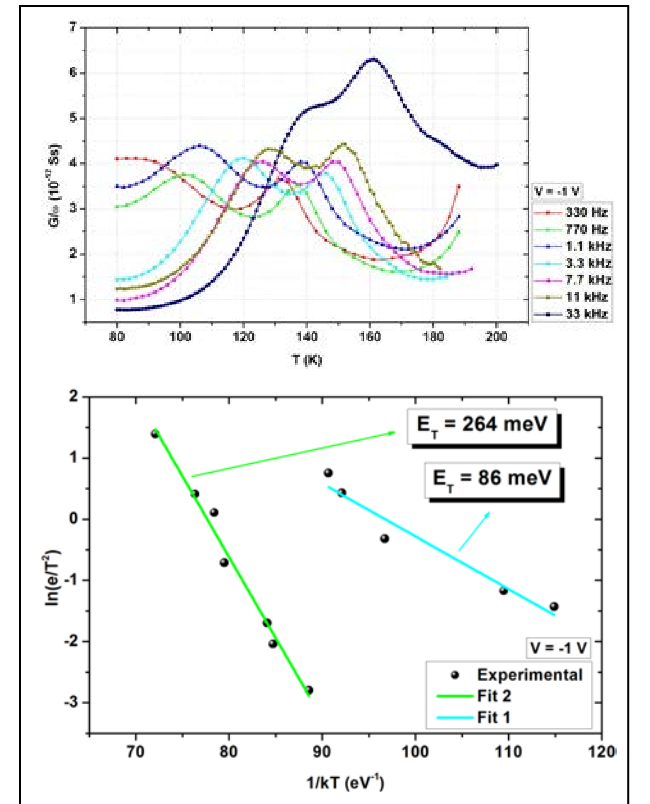

Fig.2. G/ω-T curves and Arrhenius plot for the UM2 sample biased at -1 V.

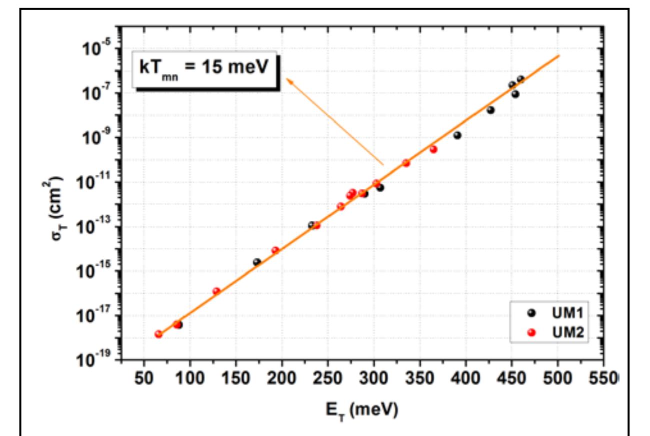

Fig.3. Capture cross section vs. activation energy at all bias values in both UM1 and UM2 samples.

Optimizing diffusion, morphology and minority carrier lifetime in Silicon for GaAsP/Si dual-junction solar cells

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The combination of III-V compounds and silicon (Si) in multijunction solar cells (MJSC) represents a long sought for device that would link the already demonstrated efficiency potential of III-V semiconductor MJSCs with the low cost and unconstrained availability of Si substrates. Among the different existing alternatives for their integration [1], currently the most developed technique is based on the direct epitaxial growth of III-V nucleation layers on Si-substrates. This approach consists on the growth of a GaP nucleation layer onto a Si substrate to obtain a III-V template free of nucleation-related defects [2-5] for growing subsequent III-V epitaxial layers. The grading of the lattice constant is achieved by a transparent step-graded $GaAs_yP_{1-y}$ buffer to shift the lattice constant to the target top cell composition (Fig. 1).

Several research groups have been working in the development of this structure. Most efforts have been directed towards the optimization of key steps in the epitaxial growth of III-V compounds on Si [3, 6, 7]. However, it is frequently overlooked that all these efforts have to be compatible with the simultaneous formation of a high quality Si subcell, which is crucial for obtaining a highly efficient III-V-on-Si MJSC. This optimization implies not only an adequate preparation of a III-V nucleation layer on the substrate for the subsequent growth, but also the formation of an emitter in the bottom subcell, while maintaining good photovoltaic (PV) properties in its base.

In our approach, the emitter is formed as a result of the phosphorus (P) diffusion that takes place during the initial stages of the Metal-Organic Vapor Phase Epitaxy (MOVPE) process. Phosphorus diffusion in crystalline silicon is a well-known phenomenon which has been thoroughly studied in the past 40 years [8]. However, the formation of the n++ emitter in the silicon subcell in a MOVPE environment is a complex process somewhat dissimilar to the traditional diffusion step in conventional PV technology. In a MOVPE reactor, the emitter is formed by the diffusion of P atoms, resulting from the pyrolysis of a gaseous source, namely PH_3, which will interact with the silicon surface. In final paper, if accepted, we will review –experimentally and using simulations– the formation of the emitter by the diffusion of P into the Si wafer. Moreover, it will be assess the role of the emitter configuration on the PV behavior of the solar cell (Table I).

A side effect of the formation of the emitter by P diffusion is the roughening of the Si surface. It has been described that exposure of Si (100) surfaces to PH_3 may result in roughening of the surface due to Si hydridation and subsequent dimmer displacement [9, 10]. Consequently, the effect on Si substrate surface morphology of the environment and conditions in the MOVPE reactor during the emitter formation will be analyzed (Fig 2). Therefore, in our quest for obtaining an optimized bottom subcell for a hybrid III-V-on-Si DJSC, we have assessed whether or not it is possible to form the emitter by P diffusion, while maintaining a high quality surface morphology on the silicon wafer. Once the emitter is formed and the surface is prepared for subsequent III-V heteroepitaxial growth, different routines have been carried out to grow a high-quality GaP nucleation layer. Important improvements have been achieved lately, as shown in Fig 3, moving from an initial 2D to a 3D growth. Nevertheless further work has to be done to achieve a defect-free structure.

In conventional Si PV technology, it is well established that the minority carrier lifetime (τ) is not a constant material property but strongly depends on the thermal history and processing environment where the solar cell is manufactured [11]. Moreover, the Si minority carrier parameters will not only govern the PV performance of the Si bottom subcell, but in turn, will also impact the entire MJSC and its optimal design [12]. Therefore, it is important to fully characterize and understand the evolution of the bulk Si minority carrier lifetime during the fabrication process used for III-V/Si MJSC structures. Accordingly, in the final paper we will report the results of a systematic study in which different environments present during the formation of the Si bottom subcell and subsequent III-V layers, influence the Si substrate bulk lifetime (Fig 4). In this respect, an initial massive reduction of lifetime is followed by a significant recovery during the III-V growth, which will be explained on the basis of H diffusion.

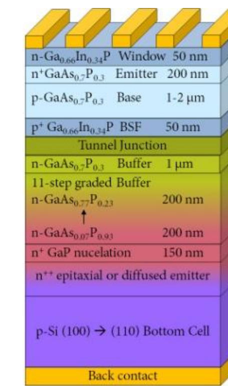


Fig 1. Metamorphic III-V on Si multijunction solar cell.

Table 1. Description of a batch of experiments where wafers were first annealed under PH_3 (step 1) and then under pure hydrogen (step 2). A comparison between simulated and experimentally measured emitter depths was established for assessing the accuracy of the diffusion model developed. Finally the PV performance of the bottom cell working on a GaAsP/Si dual junction solar cell was simulated for each sample.

		Sample 1	**Sample 2**	**Sample 3**
Step 1	Temp (ºC)	830	830	830
	Time (min)	30	30	30
	PH_3 (mbar)	32.1	32.1	32.1
Step 2	Temp (ºC)	-	830	875
	Time (min)	-	60	60
	PH_3 (mbar)	-	0	0
Emitter depth	Simulated (nm)	95-100	122-126	149-155
	Extrapolated (nm)	97-100	103-112	130-141
PV properties	Jsc (mA/cm^2)	13.898	13.898	13.898
	Voc (mV)	609.663	607.939	609.398
	FF (%)	81.282	81.353	81.293

Fig 2. Evolution of the RMS roughness (measured by AFM) during the emitter formation and subsequent surface reconstruction (by means of H_2 anneal).

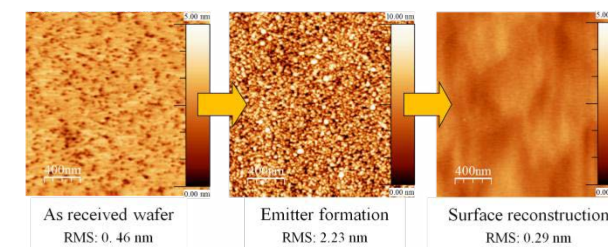


Fig.3. SEM images of a GaP layer grown on silicon following different nucleation routines.

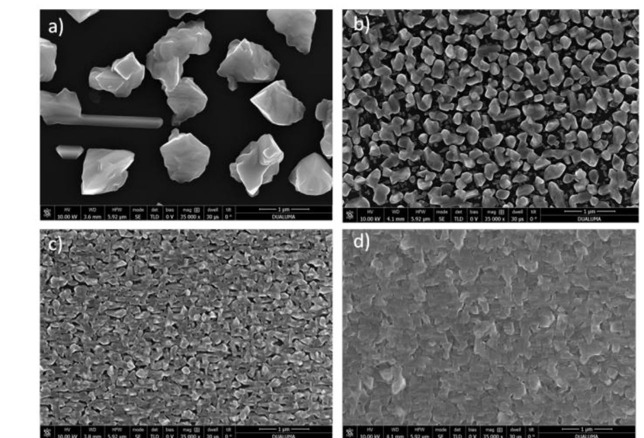
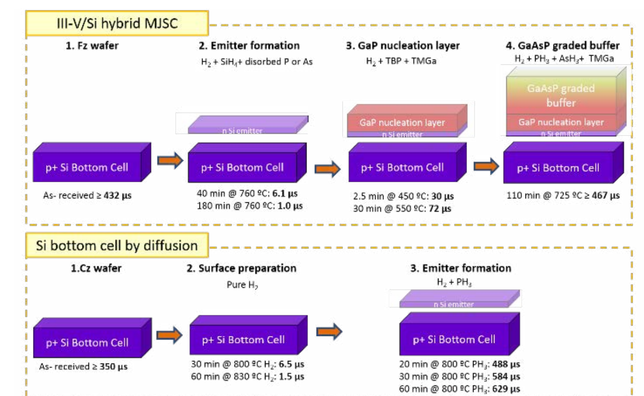


Fig.4. Evolution of average Si bulk minority carrier lifetime (top row) during the production sequence of a GaAsP/Si DJSC; (bottom row) during the formation of the emitter by P diffusion.



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Liquid characterization by means of Love-wave device combined with microfluidic platform

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1. Abstract

The aim of this work has been to develop a system with the ability to detect quickly and precisely changes in the viscosity and/or density of the liquids. For this purpose, a Love-wave device has been combined with microfluidic platform in order to work in continuous flow mode and with very small sample amounts. Different density and viscosity samples were obtained by means of glycerol-water solutions, which is a well-known lubricant. The samples were characterized by the sensor system in continuous flow and in real time, showing a fast response and a high accuracy.

2. Introduction

Viscosity and density of liquids has significant importance in many areas for different purposes. One notable example is the case of the lubricants, which must have a high quality in order to protect machinery, such as cars, turbines, ships, trains, generators and other valuable machinery. The sensor system formed by the combination of a Love-wave device with microfluidic [1,2] could be a novel and cost effective method to test the lubricants in real time by means of the density and viscosity changes, specifying the precise time to replace the lubricant.

3. Materials and Methods

A Love-wave device was used to detect viscosity and density. The Love-wave device was based on a shear horizontal surface acoustic waves propagated on ST-cut quartz and guided in a 3.5 µm film of SiO_2, being the synchronous frequency about 163 MHz. The Love-wave device was combined with a PDMS microstructured platform, and both together formed a microchannel of 150 µm of height. Comsol software was used to simulate the flow of the liquid due to microchannel shape and therefore to achieve a uniform velocity in the path between the interdigital transducers.
Glycerol had a high viscosity and density and is suitable for many sectors, such as in cosmetics or in the food or medical areas. Glycerol is also a well-known lubricant for machines that working in contact with food or medicine. Besides, it is water soluble, and thus different concentrations of glycerol in water were used in order to obtain different densities and viscosities and test the system with them (Table 1).

4. Results

Measurements of the different solutions of glycerol in water between 0% and 20% v/v were carried out at 25°C in continuous flow. Therefore, the experiment consisted of the following steps: first deionized water was introduced, then glycerol is added to a concentration of 20% and then diluted in several steps to a final concentration of 6.6% (Fig. 3). After each step the time required to reach a stable frequency was taken, which was the needed time for obtaining a homogenous solution.
The results obtained shown the ability of the system to detect in real time very low changes of the density and viscosity of the product. Besides, sensor response had a high linear behaviour of frequency shift with respect to the root of product of density and viscosity (Fig. 4).

5. Conclusions

The results have confirmed that the combination of a Love-wave device with a microfluidic platform is a novel, promising, innovative, low-cost and suitable detector for density and viscosity changes in liquids. To prove the efficiency of the presented sensor, different glycerol-water solutions were tested and high sensitivity and fast response was proved.

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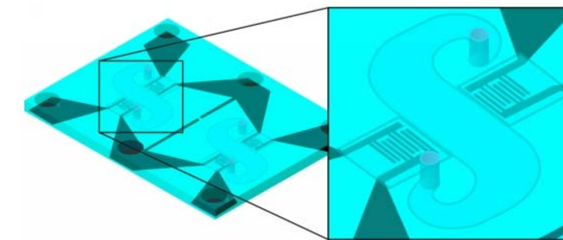

Fig.1. Love-wave device with two delay lines and a microfluidic chip of PDMS forming the two microchannels.

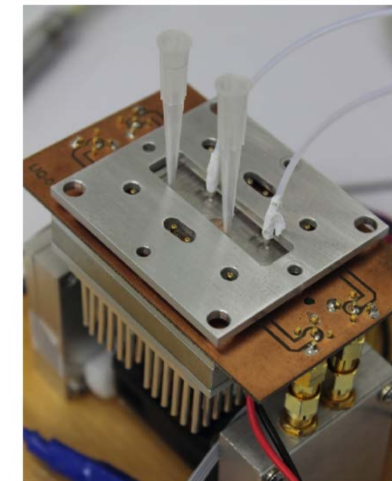

Fig.2. Tow channel microfluidic cell showing the inlet (cone) and the outlet (tube) of liquid.

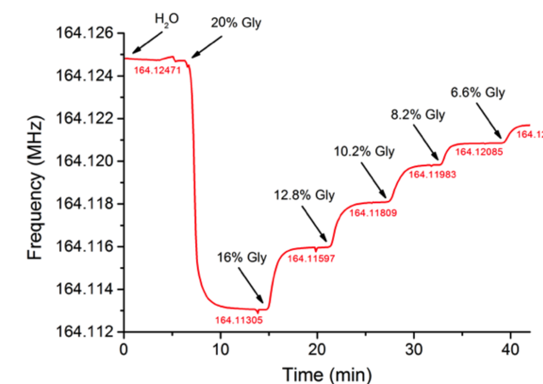

Fig.3. Real time response for different glycerol concentrations in H_2O.

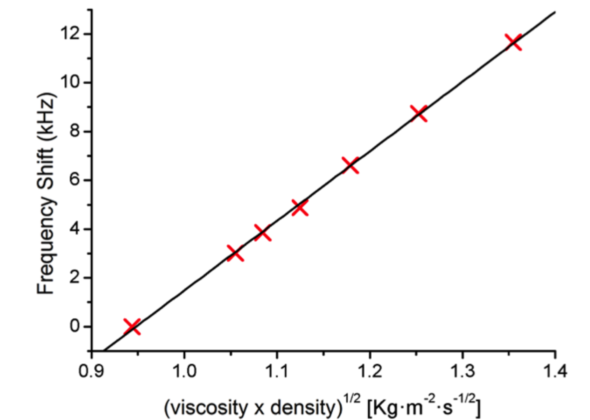

Fig.4. Linear behaviour of frequency shift vs. the square root of the product of viscosity and density.

Sample	Viscosity × 10^{-3} [N·s·m^{-2}]	Density (kg·m^{-3})
Deionized water	0.893	997
Glycerol 6.6 %	1.093	1018
Glycerol 8.2 %	1.150	1023
Glycerol 10.2 %	1.228	1030
Glycerol 12.8 %	1.339	1038
Glycerol 16.0 %	1.497	1048
Glycerol 20.0 %	1.731	1060

Table 1. Viscosity and density at 25ºC for different glycerol solutions in deionized water.

Performance of Advanced Metering Infrastructure Using Cellular Communication based on Uplink CDMA

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Abstract- This document contains sufficient information about the CDMA propagation model applied in our AMI (Advanced Metering Infrastructure), In this proposal what is intended is to study the behavior of the rate and extent implementing modeling Okumura- Hata to provide more supply, reading, cutting and re connections, prepaid services that focus on the specific characteristics of the inhabitants of rural areas and services that let you know the power consumption in real time in relation to the cost represents. The use of CDMA technology in electrical measurement systems help reduce the costs of non-technical losses and that is where we can make the most of this new system, as it would improve the quality of the electrical system getting real data readings and allowing improve communication between retailer and consumer.

Index Terms- CDMA (Code Division Multiple Access), Intelligent Networks (Smart Grid), Advanced Metering Infrastructure (AMI), diversification strategies, radio spectrum, Virtual Mobile Network Operators (MVNO) Mobile Network Operator (MNO) , primary spectrum, secondary spectrum, Long Term Evolution (LTE - Long Term Evolution), propagation model Okumura-Hata.

I. INTRODUCTION

The advanced metering infrastructure (AMI) is a banded measurement, acquisition and analysis of consumption data, this system is designed to acquire measurements of power consumption and make cuts and collections from a remote, an analysis is given more actual energy consumption nationwide, and it can give a more realistic projection of demand, additional power sector to this the possibility that the user enters into the power system as a micro generator and deliver energy under given certain conditions depending on the country where you are.[1][2]

The possibility that the user actively participates electrical system gives the advantage that governments can provide better service and support that other generators, not only in the state.[3] Smart meters are basically a static cell phone, ie it has the ability to send and receive data via wireless communication, but there is also the smart meter technology but with the possibility of a wired communication, this is achieved by distorting the wave critical noise which is interpreted as information, this information causes great harmonic distortion which should not exceed 4% of this is known as the modulating waveform.[4]

Firstly there has been replacement of analog by digital equipment electromechanical equipment as in our case: the analog meters with digital meters, communication between the supplier and consumer can make, using different technologies either CDMA; GPRS, as this technology is used more efficiently. [5]

The LTE technology was implemented in an effort to improve communication skills offered by the previous mobile networks, which is why it became the first system to provide all the packages together such as: audio, voice, data, etc., as well as [6] this model speeds exceed those obtained previously in other models coming to support at least 100 Mbps downstream and 50 Mbps for uploads; allowing us to navigate at high speeds.

Because the bandwidth of 20MHz introduce high distortions caused by the spread multica mino, we chose to use the technique of multiple access OFDMA (Orthogonal Frequency Fivision Multiple Acess) downloading or downlink, it can divide the spectrum into multiple narrow band carriers with a fixed spacing of 15 KHz. On the rise or uplink chose to use a variant of OFDMA and SC-FDMA is (Single Carrier - Frequency Division Multiple Acess) having a significant reduction in the instantaneous power ratio and average power transmitted [7][8].

Communication technology CDMA works by sharing a portion of the RF spectrum but controlling its power, this technology can be wireless or fiber optic alambica.

This type of communication focused on smart metering technology helps to cover rural areas as this type of communication is theoretically greater coverage compared to other frequencies, this leads to cutting bases and thus within the infrastructure costs.[9][10]

As shown in Figure 1 communication supplies the most remote places, this gives a clearer idea of the capacity of this type of communication.[11]

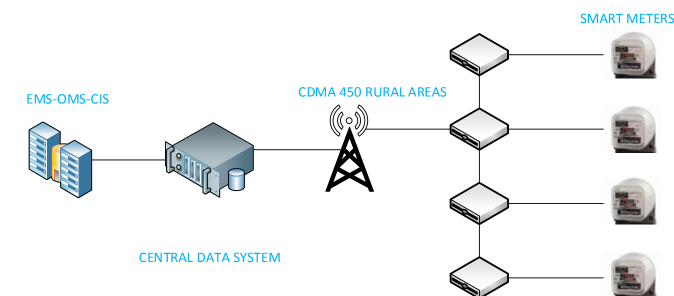

***Fig 1**. CDMA Communication*

The structure that composes a SMART GRID, we offer a high-level overview of the architecture of the intelligent network. The future power network has a layered architecture to electricity consumers. The energy starts from his generation then flows through the system continuously to transmission and distribution ultimately consumers[12].

This work carried out by a mobile virtual network operator (MVNO), which uses the infrastructure of a mobile network operator (MNO) to provide certain services to SU for the specific case are smart electricity meters being unlicensed users or those who do not acquire the spectrum under a direct grant [13][14]

The CMVNO technology as part of technology cognitive radio networks [15] [16] [17] is the key technology for a secondary user to take advantage of opportunities in a dynamic spectrum approach by detecting the spectrum. The cognitive radio is a smart radio that becomes sensitive to the context that can change its transmission parameters according to the communication environment in which it operates [18].

II. INFRASTRUCTURE FOR MEASURING POWER USING CDMA

Is the terminal access resources (radio channels) must necessarily shared

CDMA uses a spectrum by which electromagnetic energy is a signal with a wider band width, allowing a group of people connected by their cell phones generate a multiplexer on a shared bandwidth, data and voice packets , use separate codes, transmitting on different frequencies.[19]

Communication technologies for intelligent network have a lifespan of approximately 20 years without replacing components or maintenance to a very exhausted, the stability of a single communication protocol makes interoperability is something fundamental because having much manufacturers smart meters are no compatibility issues data including maintenance costs, energy consumption and installation costs are low, this makes the system has high efficiency, thus requiring a communication last mile.[19][20]

The CDMA communications with its high coverage is ideal for reaching rural air in which there is no justification to spend on infrastructure to few users. Reduce infrastructure costs of communication is one of the most important guidelines of communications today.

In Ecuador few companies have sufficient infrastructure to provide good service for communication, so renting infrastructure is vital to business communication, using wireless communications with leased spectrum allows us to access the most remote places normal spectrum provider coverage, this in order to provide service to places where neither phone arrives.
The actual measurements on each of the points of energy consumption, as we approach the CDMA communication networks to smart metering of electricity, water, gas etc ... also gives us a real projection thereof which the energy matrix a country is stable.[21]

In a few countries have designed a communications network for the use of water and natural gas, this area is virtually untouched.[1][21]

1) *CDMA 450*

In CDMA450 mathematical code is used to distinguish between multiple wireless transmit and talks. [21]

Cdma acquires a capacity of wireless transmission of high speed data delivery to customers information services from any space in which they are.[2][22]

His work on 450MHz advantage is the large signal propagation calculation could cover up to 50km. Also you can transmit to multiple users simultaneously.[23] c. [25]

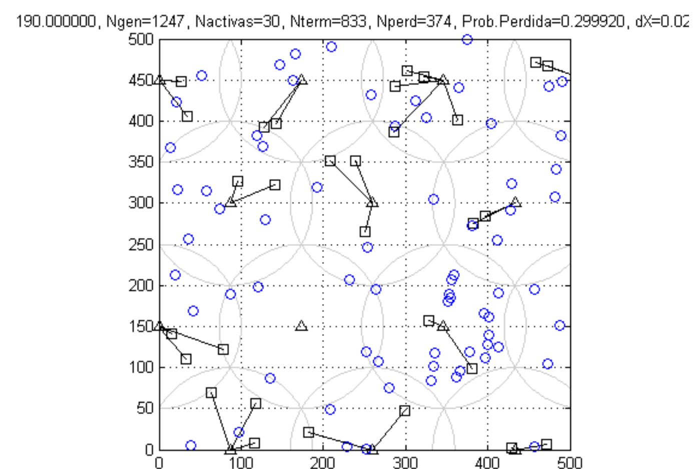

***Fig 2**. Estructura de red CDMA 450*

It has an average delay of packets of information (the time from the information block reaches the MAC layer to the physical layer). Its variance of packet delay information this is due to the delay of each packet is a random variable, has a maximum delay of packets of information which provides a life time.

Its maximum packet loss rate has exceeded the preset lifetime for them. The average rate of error in the data bits are defined either before or after encoding. The average transmission rate guaranteed in which the transmission of long intervals.

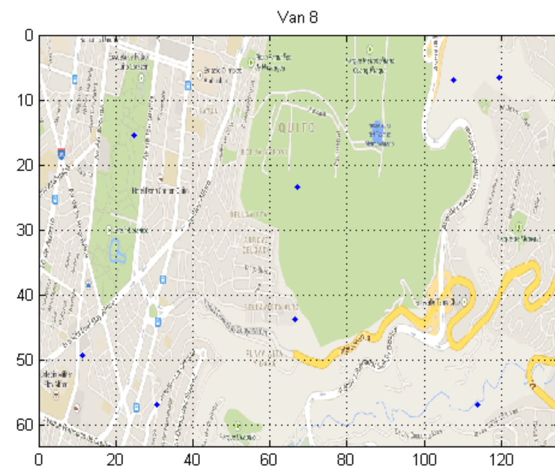

***Fig 3**. Area de cobertura de comunicación CDMA*

As is seen in the image indicate a map hacerca 45 Km clear signal arrives and the Andean part has reliefs this is perfectly applied to the person who has to go to make the delivery of payroll services and reconnection; this communication with all these activities would be avoided

III. SPREAD IN RURAL AREAS

In CDMA we have two types of channels have dogs in Downlink and Uplink.

Downlink

Downlink physical channels in the channel divided by two. A physical traffic channel is responsible for transmitting this information in shared mode and a physical control channel is responsible for establishing communication over a wireless interface, supporting communication with coats level [26]. Downlink channels have PDCCH (Physical Downlink Shared Channel), PMCH (Physical Multicast Channel), PBCH (Physical Broadcast Channel), PDCCH (Physical Downlink Control Channel), PCFICH (Physical Control Format Indicator Channel) and PHICH (Physical Hybrid ARQ Indicator Channel) [27].

Uplink

AL Like physical channels possess the Uplink Downlink physical channels and traffic control PUSCH (Physical Uplink Shared Channel), PUCCH (Physical Uplink Control Channel) and PRACH (Physical Random Access Channel) [27].

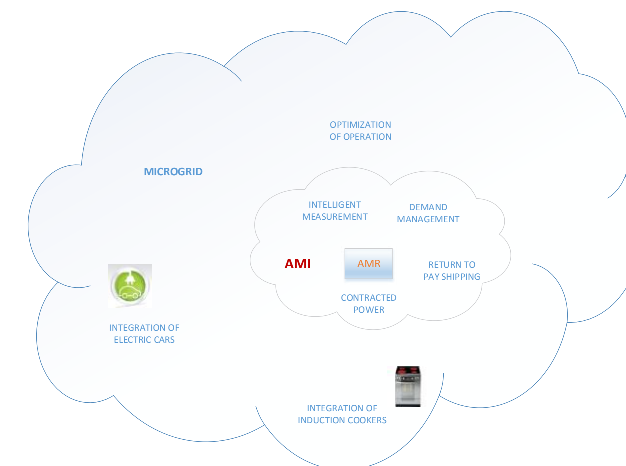

***Fig 4**. Scope of smart metering systems.*

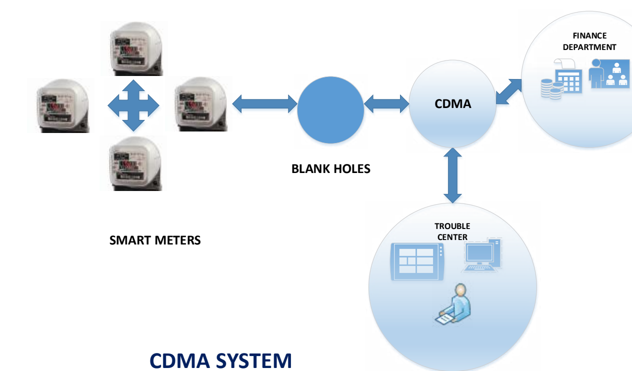

***Fig 5**. Infrastructure AMI – CDMA system*

IV. MODEL OKUMURA-HATA

Which is an empirical model that is applied to cities and rural areas based on measurements in Tokyo, presents the additional attenuation in free space, Soft Ground and urban environment is not based on any physical model curves for frequencies 150-1500 MHz, and smooth curves for rugged terrain, antenna height approx RB. 200 m.

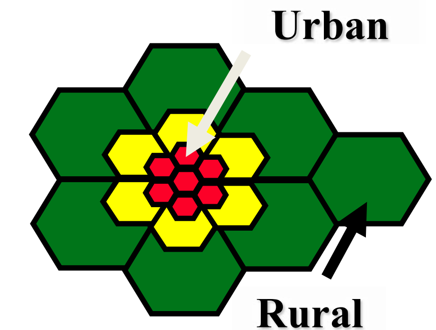

***Fig 6**. Identifying areas*

The following equation can calculate the QUALCOMM CDMA

$$N = \frac{S}{R}\cdot\frac{1}{\frac{Eb}{No}} + \frac{1}{V}.F.C$$

Where:
N = Calls Per Cell...................Assuming: Rayleigh Fading Reverse Link
S = Spread Spectrum Bandwidth........................Assuming: 1.25 MHz
R = Data Rate in Kbps...ssuming:9600 bps
Eb/No = Bit Energy+ Noise Power Spectral Desity......Assuming: 60 dB
V = Voice Duty Cycle..Assuming: 50%
F = Frequency Reuse Efficiency.....................................Assuming: 60%
C = Number of Sectors in Cell....................Assuming: 3 sectors (120º)
Radio Capacity Per Cell.......................120 CDMA Channels in 1.25Mhz
Erlang Capacity Per Cell (2% Blocking).............107 Erlangs in 1.25Mhz

Applying the maximum of the resulting equation gives approximately 190 000 call per cell as shown in Figure 2, which can apply if all users are in service with smart meters.

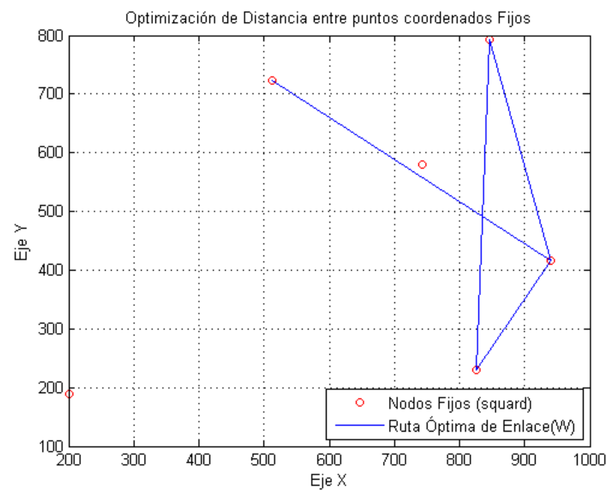

***Fig** 7. Spread CDMA communication coverage*

V. CONCLUSIONS

The main conclusion a smart grid (Smart Grid) for Advanced Metering Infrastructure (AMI) would be a good concept for a more feasible and convenient for the user and the server worked.

The CDMA technology is booming for some time in most countries. The implementation of intelligent networks for various purposes is endless and very appealing.

The propagation model Okumura-Hata works for calculating propagation in urban areas is a radio propagation model, which was constructed from data collected in the city of Tokyo, Japan. The model is ideal for use in cities with many urban structures, but not many of the structures of high insulation. The model was the basis for the Hata model. Okumura model was built in three modes, suburban, and urban open. The model for urban areas was constructed and used as the basis for others.

By comparing the benefits of AMI AMR over its predecessor is analyzed. In this paper, an analysis of infrastructure and communication technologies used by AMI presented.

Communications based on radio frequency or cell phone have high expectations for robustness, multiple bandwidths and capabilities to coexist in the same spectrum depending on the specific needs of the sector.

Smart Metering, AMI and communication systems are working basis for distributed generation. By reusing the cellular network infrastructure, there is a large reduction in costs; as smart metering does not exceed network capacity and allows billed only for the data obtained in the energy meters either GPRS or CDMA is used.

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BIOGRAPHY:

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On the ageing mechanisms of graphene electrodes

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1. Abstract

Graphene electrodes are being massively introduced in a wide range of electronic devices[1]. On the contrary, exhaustive ageing studies, which are necessary prior to device commercialization, have never been performed before. This paper presents the first complete reliability study of a carbon-based electrode, and the main ageing mechanisms are discussed. We use accelerated ageing tests and nanoscale and device level experiments, as well as Weibull statistical analyses and Fowler Nordheim and Direct Tunneling simulations.

2. Characterization tests

Graphene single layer (GSL) sheets grown on copper by chemical vapor deposition are subjected to accelerated oxidative tests by immersing them in hydrogen peroxide (H_2O_2) for different times, which produces a degree of oxidation similar to months in room atmosphere[2]. After the treatment, the samples are analyzed with optical microscope, scanning electron microscope (SEM), conductive atomic force microscope (CAFM), X-ray photoelectron spectroscopy (XPS), Raman spectroscopy and ultraviolet-visible spectrophotometer (UV-VIS). The CAFM current-voltage (IV) curves have been fitted to the combined Fowler Nordheim - Direct Tunneling (FN-DT) equation (not shown) to assess the EOT of the samples (physical thickness of a thin SiO_2 stack with similar electrical properties). The ageing of the GSL sheets is studied in real devices through single back-gate GFET fabricated by electron beam lithography, electron beam evaporator and lift off.

3. Nanoscale characterization

After the oxidative treatment, we measure the UV-VIS signal for fresh and soaked samples. Fig.1 shows the transparency of the GSL sheet decreases drastically with the treatment time. XPS data in Fig.2 indicates an increase of the oxygen in the treated sample. We collect AFM topographic maps on the surface of the sample, and we process the images offline with the software to assess the amount of area oxidized (covered by hillocks). We observe that after 4h the oxidation phenomenon saturates to a value of ~25% (Fig.3).

The local conductivity of the samples is analyzed by means of IV curves and current maps collected with the CAFM at random locations of the samples. Fig.4 shows the IV curves collected on the samples treated for different times. After 1h treatment, a group of IV curves show Ohmic conduction similar to fresh samples, while the rest shows larger onset voltage corresponding to partially oxidized locations (Schottky). EOTs up to 1.8 nm on pristine graphene and up to 6nm on graphene defects have been obtained fitting the IV curves to the FN-DT equations. After 4h treatment, no signal of Ohmic conduction has been detected anymore (Fig.4b), indicating that the whole surface of graphene has been oxidized. Oxidation became critical after 10h, and the currents were dramatically reduced (not shown).

4. Device level performance

After 4h treatment in H_2O_2, GSL sheets have been transferred onto 300 nm SiO_2/Si wafers, metallic pads have been patterned, and the GSL channel delimited (Fig.5). Fig.6 compares the performance of GFETs with fresh and pre-oxidized channels. While fresh ones show the typical current increase (until a maximum current density in which the channel physically breaks by electromigration), treated ones show three types of degradations: first, the initial zero-current at low voltages below 2.5V (black arrow) indicates that the graphene sheet may be completely oxidized at some locations (producing an onset voltage effect; second, the sudden current increase around 7V (green arrow) could be related to the breakdown of some oxide by thermal heat; and finally, we observe a considerable reduction of the voltage at which the graphene electrode physically breaks (orange arrow).

5. Conclusion

Our experiments and calculations reveal that the main two ageing mechanisms of graphene electrodes are: i) the formation of an ultra-thin oxide layer on pristine graphene; and ii) the formation of tall oxide hillocks at graphene point defects. Such layer is observed to change the conduction mode at the interface (from Ohmic to Schottky), and can lead to premature failure in real graphene field effect transistors (GFET).

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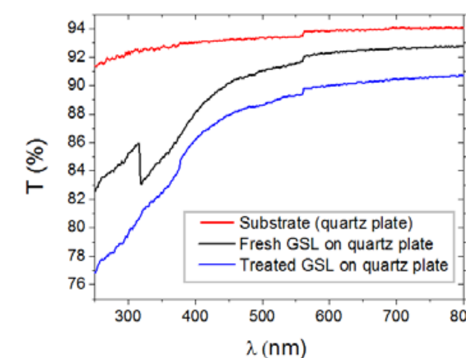

Fig.1. UV-VIS analysis of the GSL/Cu stacks, fresh and treated in H_2O_2 for 10h. Treated samples experience a reduction of the transparency.

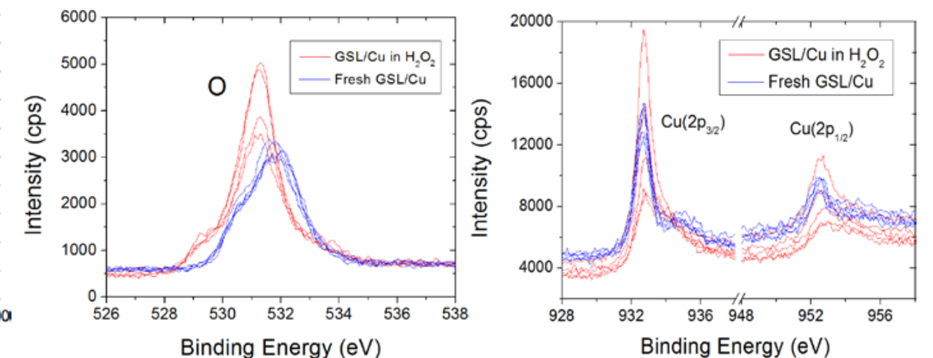

Fig.2. XPS analysis of fresh and treated (10h) GSL/Cu stacks. The content of Oxygen is larger in the treated sample, and the deviation of the Cu peaks is also larger, indicating a more inhomogeneous structure. The Cu peaks are broader in the treated sample, suggesting the formation of Cu_2O, CuO and $Cu(OH)_2$ peaks.

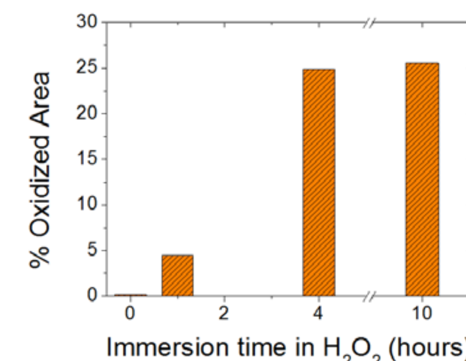

Fig.3. Analysis of the area oxidized depending on the treatment time (calculated form AFM maps). After 4h the oxidation saturates.

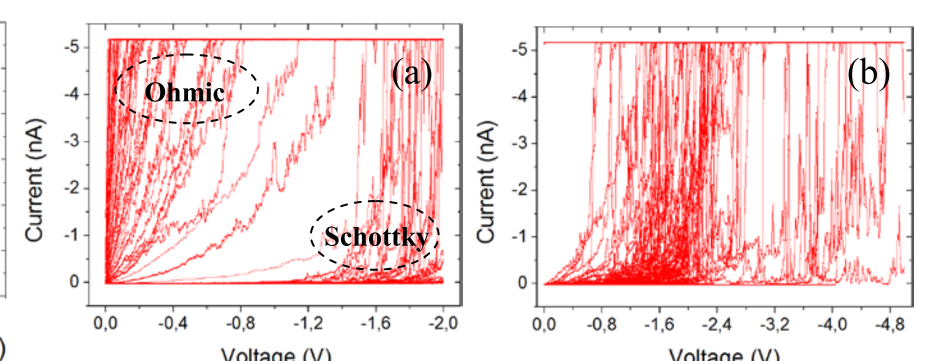

Fig.4. IV curves measured with the CAFM at random locations on the surface of the samples treated in H_2O_2 during 1h (a), 4h (b). Ohmic contact vanishes with the time, and the IV curves show Schottky conduction.

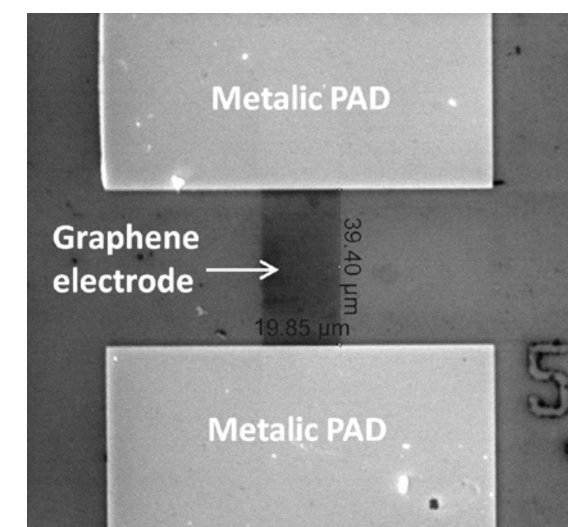

Fig.5. SEM image of a GFET with a pre-oxidized channel. First, the GSL sheet was treated in H_2O_2, and later the transistor was fabricated by electron beam lithography, electron beam evaporator and lift off. The currents were measured in the probestation.

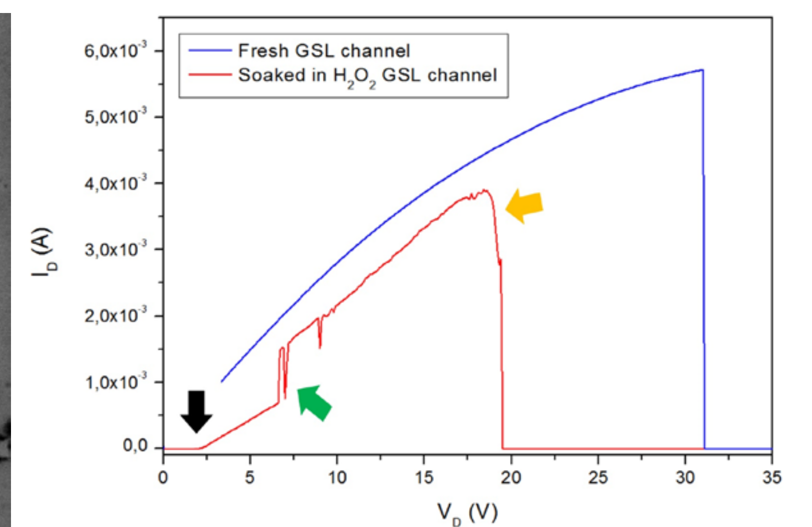

Fig.6. Drain current vs. drain voltage curves for fresh and treated GSL sheets. In treated samples three degradation effects have been observed: onset voltage (black arrow), current fluctuations (green arrow) and premature breakdown due to electromigration (orange arrow).

In situ TEM study of reduction of graphene oxide by Joule heating

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1. Introduction

Graphene has attracted a great interest from scientists due to its intrinsic mechanical, thermal and electrical properties [1]. The excellent properties of graphene [2] have driven the search for methods for its large-scale production.
The oxidation-reduction method is considered one of the most attractive methods to obtain graphene because it is cheaply scalable and versatile. Graphene oxide (GO) contains saturated sp3 carbon atoms bound to oxygen, which make GO non-conducting [3]. There is, thus, a growing interest in monitoring the reduction process of GO sheets into reduced graphene oxide (rGO). Besides, the thermal annealing reduction of GO removes the oxygen-containing groups bonded to the graphene and removes other atomic-scale lattice defects which can increase the conductivity several orders of magnitude [4], [5].

2. Procedure

In this work, GO, produced using a slight modification of the Hummers oxidation method from natural graphite flakes [6], has been in situ reduced by Joule heating in a JEOL 2100 Transmission Electron Microscope (TEM) equipped with a Scanning Tunneling Microscope (STM) used as an in situ TEM electrical probe. Figure 1 shows a schematic of the TEM-STM system used in this experiment.
The procedure for this experiment consists of applying a bias of 5V to a GO nano-platelet during 1 minute in order to achieve a Joule heating above 2000ºC[7],[8], a temperature high enough for the reduction of GO[9],[10]. The thermal annealing of the GO nano-platelet is meant to remove the O-containing groups and reduce the sample. Besides, to measure the resistance of the sample before and after the thermal annealing a 100ms voltage ramp from -1V to +1V is applied.

3. Results

The reduction of GO has been measured qualitatively from the comparison of conductivity of the sample before and after the reduction, all in the same experiment. Besides, with this technique it is possible to control the reduction from the measure of the conductivity of the sample and also characterize the sample during the experiment (both through TEM observation and through current-voltage characteristic).
Figure 2 shows the TEM image of the GO nano-platelet before and after reduction and its electrical characterization. Both images show the platinum tip contacting the GO nano-platelet attached to the TEM copper grid. There were no observable changes in the geometry of the sample or in the tip-sample contact.
Indeed, the results show how GO has been reduced by observing a decrease of the resistance of more than four orders of magnitude. Finally, the results obtained for the resistance of both GO and rGO are comparable with results from literature[9],[11],[12].

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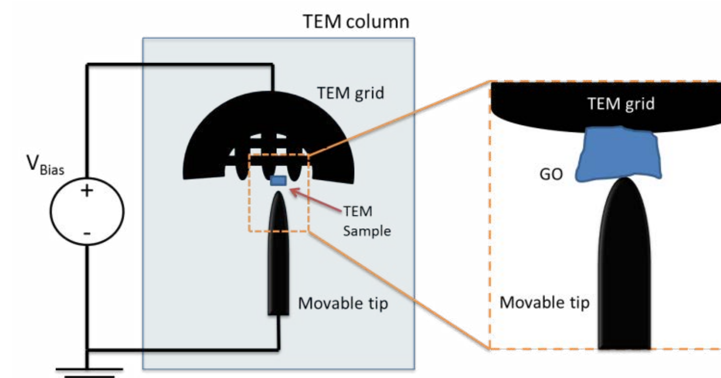

Fig.1. Schematic of the experiment configuration with the TEM-STM system.

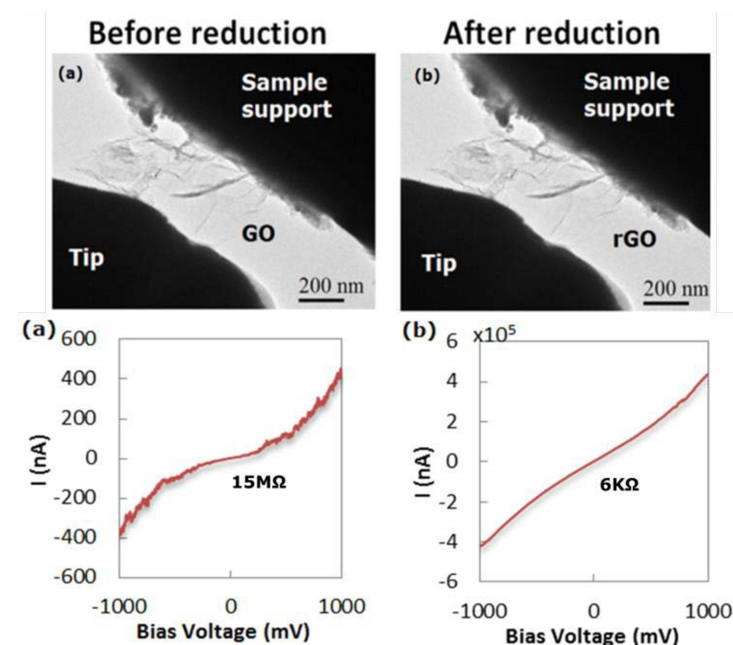

Fig.2. TEM images of the GO nano-platelet before and after reduction and its electrical characterization.

Low dose radiation effects on a-Si:H TFTs

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1. Abstract

In this paper we analyze the effects of X-ray irradiation on a-Si:H TFTs. We have irradiated at low doses, up to 1 krad, and we have measured several transistors, obtaining coherent behaviors. The main effect is a shifting of the threshold voltage, as well as a change in the Ioff current and a change in the mobility. We discuss these effects, and found them to be around three orders of magnitude higher than in an equivalent bulk CMOS technology.

2. Introduction

The low process temperatures required for polysilicon TFT's fabrication, together with the possibility to integrate relatively complex circuits, makes them highly suitable for driving flat panels displays such as LCD and, more recently, AMOLED. Since these displays could be used in scenarios with radiation hazard, such as hospitals or nuclear research laboratories, or purposely as radiation detectors, like the flat panel X-ray imaging aiming to replace film and chemicals in radiography, it is necessary to fully characterize its radiation response. Although many authors [1, 2] have studied the radiation effects on TFT's, quantitative and qualitative resultsare different for each fabrication process. Therefore, each technology requires a specific characterization.

The purpose of this paper is to determine the effects related to the X-ray total ionizing dose in a particular a-Si:H TFT technology.

3. Experimental Setup

The back channel etched a-Si:H bottom-gate TFTs were fabricated using laboratory facilities of the Giga-to-Nanoelectronics Centre at the University of Waterloo, Canada. The TFT process started with the deposition of a 80nm Cr by sputtering to pattern the bottom-gate metal. Next, a tri-layer of 350nm a-SiN:H gate dielectric, 150nm a-Si:H channel, and 60nm n^+a-Si:H ohmic contact layers was consecutively deposited at 170°C using 13.56MHz PECVD. After patterning the TFT active area using dry etching, a 100nm Cr as source/drain metal was sputtered and patterned. Then, the n^+a-Si:H was etched using dry etching to define the effective channel region, followed by the deposition of a 350nm passivation a-SiN:H layer at 170°C using the PECVD and then by opening via for contacts. The TFTs fabricated were annealed in air at 150°C for 2 hours before the measurements.

The fabricated TFTs were characterized in the University of the Balearic Islands, and after the initial measurements, they were irradiated using X-rays. The radiation field is 20x20 cm, and the dose rate is 100rad/s. The circuits were irradiated for 5 minutes allowing a total dose of 500 rads in each irradiation, and were afterwards annealed in air at room temperature for one week before measurement.

4. Results and discussion

Figure 2 shows a sample of the measured I-V transfer characteristic curves. We have represented the measured curves for the three measured cases: non irradiated transistor, 0.5 krad, and 1.0 krad. It is apparent that there is a change in the threshold voltage, as well as a change in the slope of the curve in the over threshold region. It is not shown in the figure, but there is also a raise on the Ioff current.

The change in the threshold voltage can be explained by the accumulation of charges in the gate oxide, while the change in Ioff is attributed to changes in the substrate. The change in the slope of the curve is, probably, due to changes in the trap energy distribution, which affect directly to the mobility.

The above changes have been evaluated for several transistors, and the estimated rates of change are given in table I. It has to be noticed that these rates of change suffer a certain dispersion, that can be attributed to differences in the transistors (i.e. different roughness of the oxide-semiconductor interface, variable thicknesses, etc….) caused by the fabrication process.

To put these variations in perspective, we can compare them with those suffered by a CMOS technology old enough to be equivalent, as published in [], where the effects of up to 2 Mrad doses were evaluated. The results show that the threshold voltage in the TFTs under 1 krad dose experiment variations equivalent to those in the CMOS technology under 1 Mrad dose. Thus, it seems that this specific a-Si:HTFT technology is much more sensitive to radiation than conventional (bulk) CMOS. It must be noted that radiation effects on the threshold voltage in recent technologies are greatly reduced, because of the shrinking gate oxide.

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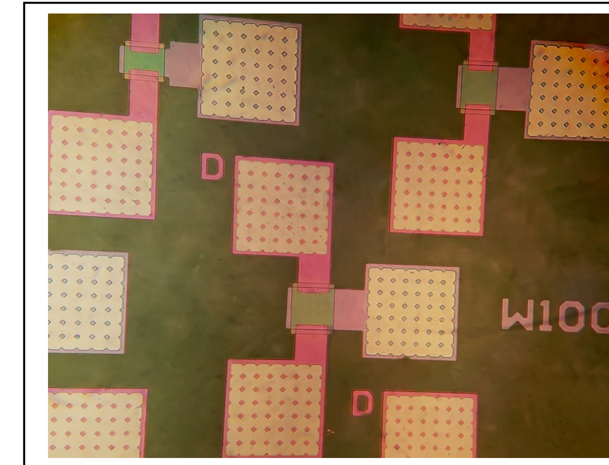

Fig.1. Photography of the measured TFTs. Only some of the measured samples are shown.

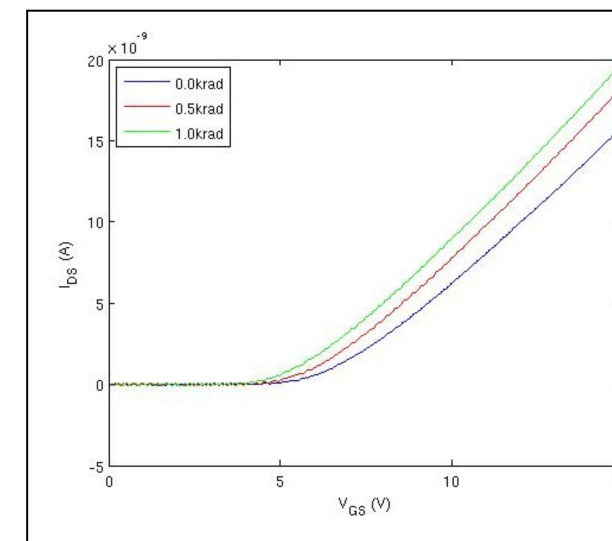

Fig.2. Transfer characteristics of the W/L=100um/100um transistor for the three measured cases: non-irradiated (0 krad), 0.5 krad and 1.0 krad.

Parameter	Nominal value (0 krad)	Variation (units/krad)
V_{th} [V]	5.4 ± 0.7	-1.06 ± 0.36
I_{off} [pA]	26.3 ± 2.7	8.5 ± 3.8
γ [−]	0.18 ± 0.06	-0.05 ± 0.03

Table1. Nominal (non irradiated) values for the evaluated parameters, along with the estimated linear changes due to radiation, and their estimated dispersion margin.

SiNERGY, a project on energy harvesting and microstorage empowered by Silicon technologies

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1. Abstract

Internet of Things and Trillion Sensors are buzzwords illustrating the path towards the next grand paradigm: Smart Everywhere. In many of those realizations long term autonomy of sensor systems is a must to tackle different societal challenges and innovation scenarios. Microenergy autonomy solutions based on energy harvesting offer a promising way in which, KETS mediated, silicon technology and silicon friendly materials may play a decisive role.

2. Project description

Micro and nanotechnologies have already made possible the fabrication of small, low cost and good performance sensors that are called to be protagonists of continuous monitoring scenarios and distributed intelligence paradigms. Energy autonomy keeps being one of the most desired enabling functionalities in the context of off-grid applications, such as wireless sensor networks. In many such applications, wired power is not feasible and batteries are normally used. However, battery replacement will eventually become impractical (economically, environmentally, and logistically) not only for sensor networks in remote places or harsh environments, but also for more standard applications if the number of nodes explodes exponentially.
Harvesting energy, tapping into environmentally available sources such as heat and vibrations, may be a good solution in man-made scenarios applications. Energy densities of 100µW/cm2 seem appropriate for many such applications. Furthermore, coupling those harvester devices to secondary batteries to buffer enough energy to account for the power demand peaks required by the communication unit of wireless nodes could be a quite enabling energy autonomy solution.
SiNERGY, a recent EU project, focuses on silicon and silicon friendly materials and technologies to explore energy harvesting and storage concepts for powering microsensors nodes. Silicon technologies provide an enabling path to miniaturization, 3D architectures (improved energy densities), mass production with economy of scale, and the ability of power intelligence integration. Being silicon technologies the ones used for the fabrication of the sensors themselves, they are the prime candidate for building microenergy solutions of similar robustness able to power such sensors during their whole lifetime.

Within the project different approaches for thermal harvesters, mechanical harvesters and thin film/3D solid state batteries are considered. An exploding number of sensors makes small sensor size desirable. Their microenergy companions are then also under a downscale pressure. Energy harvesting sources tend to be low energy density sources. Capturing enough energy in such conditions demands architectures with high density features. Silicon micronanotechnologies offer the possibility of micromachining, which produces free surfaces and volumes that can couple with the environment, and quasi 3D architectures with high aspect ratios, into which nanomaterials may be integrated if need be, thus enabling such internal high density features. Examples of some of the proposed devices architectures and bottom-up or top-down nanomaterial integration will be shown and discussed

Acknowledgement. This work was supported by FP7-NMP-2013-SMALL-7, SiNERGY (Silicon Friendly Materials and Device Solutions for Microenergy Applications), Contract n. 604169

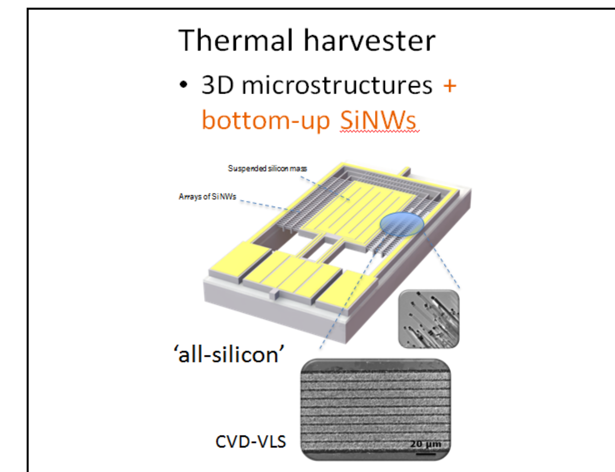

Fig.1. Example of a 3D silicon microplatform for a thermoelectric device integrating bottom-up silicon nanowires as thermoelectric material

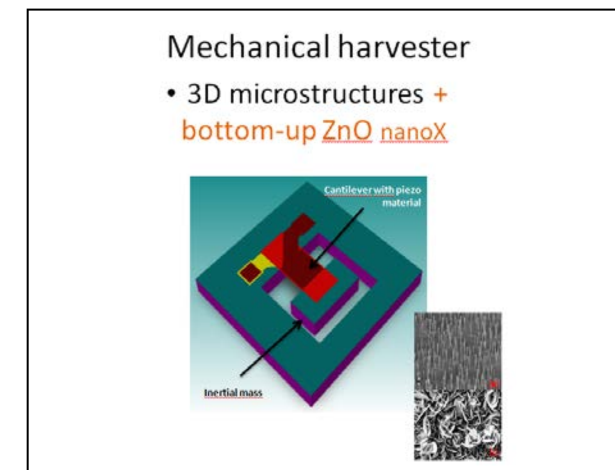

Fig.1. Example of a 3D silicon microplatform for a mechanical harvesting device integrating bottom-up piezoelectric nano-objects

DC SHEs on GaN HEMTs varying substrate material

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1. Abstract

In this paper DC characteristics of an AlGaN/GaN on sapphire high-electron mobility transistor (HEMT) are measured, numerically simulated, and modelled accounting for self-heating effects (SHEs), with the main electrical parameters being extracted. By decomposing the transistor thermal resistance into the buffer and substrate components we extend our study to substrate materials other than sapphire (Si, Mo, SiC). Furthermore, we implement a compact model available for AlGaN/GaN HEMTs, including the temperature dependence of extrinsic source/drain ohmic resistances, which are numerically evaluated for different substrates.

2. Introduction

Substrates with a high thermal conductivity are desirable in HEMTs, because most of the internal heat is spread out through the substrate. Sapphire has been the main substrate used in optical GaN-based devices. However, advancements in technological manufacturing processes have allowed alternative materials, with better thermal conductivity, to be employed in high power electrical applications. Nevertheless, several questions on behaviour and reliability need still to be answered.

3. AlGaN/GaN on Sapphire HEMTs

We characterize, experimentally and numerically, the DC performance of AlGaN/GaN on sapphire HEMTs, the layer stack of which is shown in Fig. 1; semiconductors were grown through the [0001] direction (wurtzite) on 330-μm-thick sapphire.

All measurements have been performed within a KARL-SUSS Probe Station at the ISOM-UPM lab. For the *C–V* characteristics, a mercury microprobe with an area of 4.24×10^{-3} cm^2 and the HP41992A-LF Multi-Frequency Capacitance Measurement Unit were used. DC characteristics have been measured with the HP4145B Semiconductor Device Analyzer.

Numerical simulations have been performed with ATLAS (from Silvaco) [1]. First, in order to reproduce the DC HEMTs response, with mobility and saturation velocity parameters of Table 1, the electron profile through heterojunctions has been established from the *C–V* characteristics [2] (see Fig. 2). For that purpose, the piezoelectric and spontaneous polarizations are incorporated. No trapping effects, dislocations, or surface states [3] are considered in this work, which are compensated assuming 60% of the polarization charge.

The drain current of the AlGaN/GaN on sapphire HEMTs is modelled using the simple compact analytical model presented in [4] which is based on semiconductor physics, covers all the different operating regimes, and is given by:

$$I_{ds} = -\frac{q\mu W}{L}\left[\frac{qd}{2\varepsilon}\left(n_D^2 - n_S^2\right) + \frac{2}{5}\gamma_0\left(n_D^{5/3} - n_S^{5/3}\right) + V_{th}\left(n_D - n_S\right)\right] \quad (1)$$

The model accounts for channel length modulation, short channel and self-heating effects, and incorporates the temperature dependence of extrinsic source/drain ohmic resistances, ($R_{s,d} = a + b\cdot T + c\cdot T^2$) which are numerically evaluated and modelled with parameters of Table 2. The resulting measured, simulated and modelled output characteristics are successfully compared in Fig. 2.

4. SHEs varying substrate material

Once numerical simulations and modelling of the sapphire HEMTs DC characteristics have been successfully validated, the impact of SHEs when the substrate material is varied is analyzed with ATLAS. For that purpose, technological dependent parasitic effects such as trapping, dislocations, or surface states, are assumed to contribute similarly to the measured HEMTs for deriving similar 2-DEG concentration, threshold voltage, and (temperature dependent) electron mobility in buffer and barrier layers. This includes similar passivation layers on top of the barrier, and similar terminal layout.

By employing the corresponding device thermal resistance, we obtain the numerical output characteristics of Fig. 4 for sapphire, SiC, and Si or Mo (they overlap) substrates, for null gate bias to enhance SHEs, which have been also successfully modelled. The corresponding transistor performance with maximum overheating (for V_{ds} = 15 V) is indicated in Table 3.

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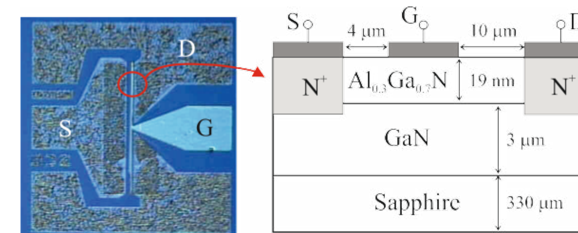

Fig.1. AlGaN/GaN on sapphire HEMTs structure (not to scale) and layout microphotograph.

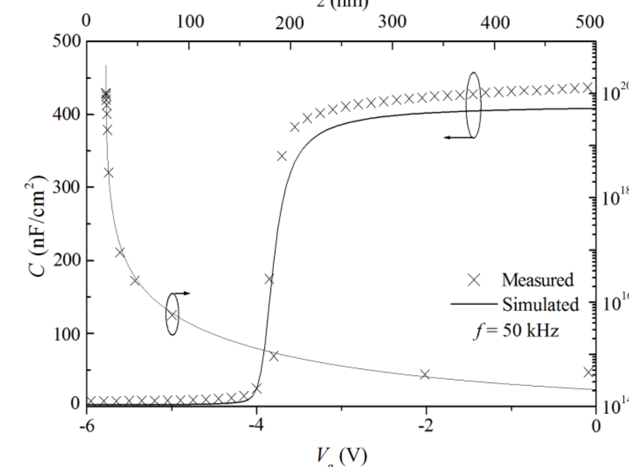

Fig.2. *C-V* characteristics (left axis) and electron profile against the depth from the AlGaN top surface (right axis). Measured and simulated data are represented with crosses and solid lines, respectively.

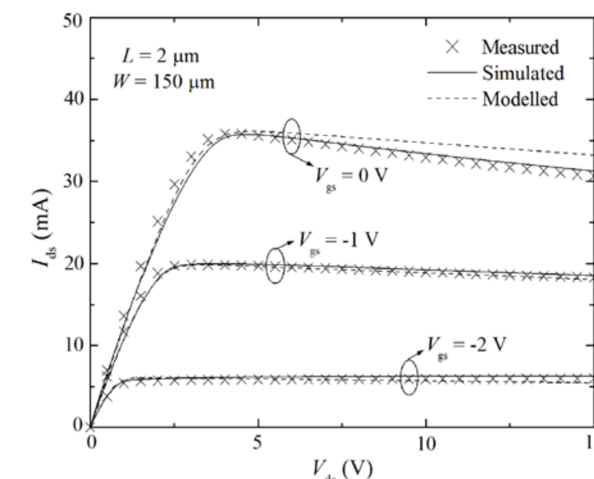

Fig.3. Sapphire HEMTs output characteristics. Measured, simulated, and modelled data are represented with crosses, solid lines, and dashed lines, respectively; Vgs (V) = –2, –1, and 0.

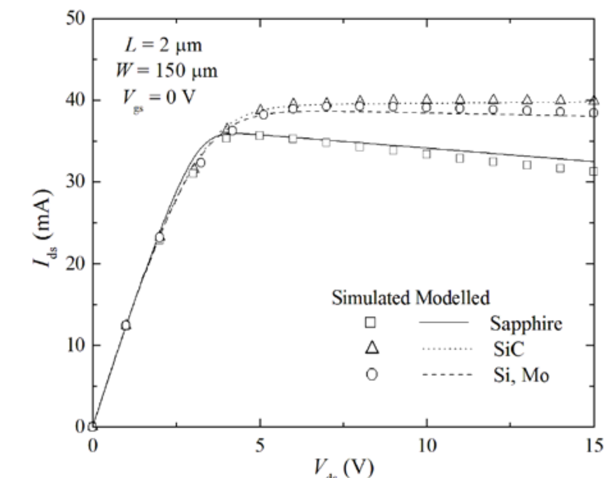

Fig.4. Output characteristics for sapphire, SiC, and Si or Mo substrates (Si and Mo data are fully overlapped). Numerical data are represented with squares, triangles, and circles, and modelled data with solid, dotted, and dashed lines, respectively.

	GaN	AlGaN
μ_{max} (cm^2/V-s)	900	940
$v_{sat,o}$ (cm/s)	10^7	10^5
$v_{sat,d}$ ($\times10^6$ cm/s-K)	1.2	1.2
α	1.5	1.5
β	1.6	2.0

Table 1. Mobility and saturation velocity parameters for the GaN buffer and $Al_{0.3}Ga_{0.7}N$ barrier.

	Sapphire		Si/Mo		SiC	
	R_s	R_d	R_s	R_d	R_s	R_d
a (Ω)	0.07	29	15.6	137	15	245.3
b (Ω/K)	0.03	0.05	1.6×10^{-4}	–0.7	3.2×10^{-5}	–1.4
c ($\times10^{-3}$Ω/K^2)	–	0.14	–	–1	–	2.5

Table 2. Fitting parameters for R_s and R_d with substrates.

Substrate	$T_{l,max}$ (K)	$<T_l>_{max}$ (K)	$I_{ds,max}/W$ (mA/mm)	$g_{m,max}$ (mS/mm)
Sapphire	467	435	239	86
Si/Mo	381	357	262	118
SiC	357	332	267	120

Table 3. DC numerical performance parameters with substrates and maximum overheating (V_{gs} = 0 V, V_{ds} = 15 V).

Feasibility of dispensing technology to create local contacts on silicon solar cells

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1. Introduction

Thin silicon wafers are a way to reduce costs in the raw material, but the bowing of such wafers after metallization causes its breaking in most of the cases and also *microbreaks* in the structure affecting to the lifetimes and to the efficiency of the final solar cell. This effect can be reduced by using non-contact metallization techniques like dispensing technology as many authors reported for obtaining the front electrodes with silver paste [1,2].

In this work we present a microstructural and electrical characterization of aluminum structures obtained after the dispensing printing of different aluminum pastes on monocrystalline p-type silicon substrates, followed by firing of that pastes with the aim to obtain rear contacts for silicon solar cells.

2. Materials and experimental

The robot used to carry out the dispensing printing (drop on demand technique) was the model F7900N from Fisnar. The main unit was connected to a 'teach pendant' (Fig. 1) and to the frequency unit to supply the air at chosen pressures.

Before programming the robot to dispense a dot of material, the dispensing nozzle must be jogged to the desired XYZ location. When a program is set, the series of instructions are stored in the main unit memory and each instruction is stored in a numbered memory address. When a program is run, the robot steps through each memory address in sequence and execute the instruction found there.

In this work, lines of two different aluminum pastes named T1 and T2 from Toyo Aluminium K. K. were obtained by the printing of very close dots so that the final appearance was a line. The instructions sent to the robot to run the program are described in Table 1. After printing, the samples were dried at 250 ºC and then fired in a tubular furnace at 950 ºC. Contact resistance was calculated from the resistance values obtained by TLM (Transmission Line Measurement) and the diffusion of aluminum in the silicon was checked by FESEM pictures.

3. Results and discussion

The two aluminum pastes used to create a local back surface field on silicon wafers have <10% weight of lead-free frits and the mass deposited is described in Table 2. Contact resistance was calculated and compared between the different pastes and optical and FESEM pictures were taken as well to check the formation of the LBSF (Local Back Surface Field).After a firing at 950 ºC the optical microscope was used to take pictures of the obtained structures on as-cut silicon wafers using the two aluminum pastes and a 150 µm diameter nozzle (Fig. 2). The lines remain attached to the silicon substrates in the two cases. The FESEM image shown in Fig. 3 exhibits a cross-section for a line obtained with paste T1, carried out without insert the sample in any resin. The thickness of the eutectic layer formed after the firing was measured by FESEM and took a value of 35.09 µm and 103 µm for paste T1 and T2 respectively, which were in accordance with the values of specific contact resistivity shown in Table 3. The more the eutectic layer became, the more the contact between aluminum and silicon and the less the contact resistivity.

Summing up, this method allows the formation of local contacts in silicon wafers allowing the creation of a LBSF, reaching a best value of specific contact resistance of 54 mΩcm^2 for paste T2, which is similar to other values for samples obtained by screen-printing [3].

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Acknowledgements

The authors are grateful to MINECO of Spain for the financial support received through the project TEC2010-16700.

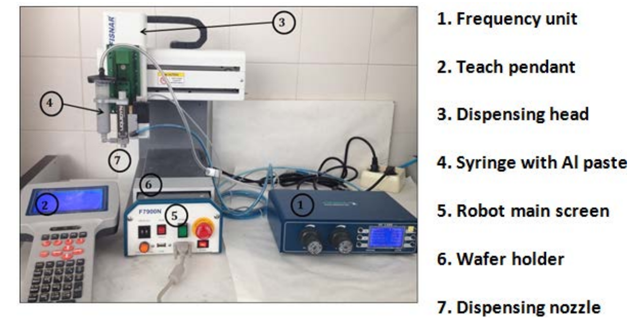

Fig.1. Dispensing printing equipment

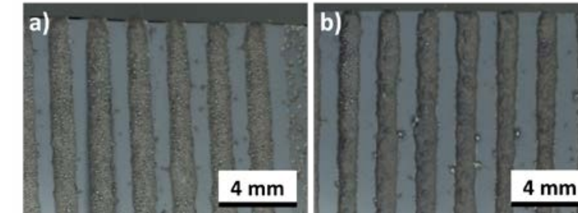

Fig.2. Optical microscope images for lines created on as-cut silicon substrates with pastes T1 (a) and T2 (b).

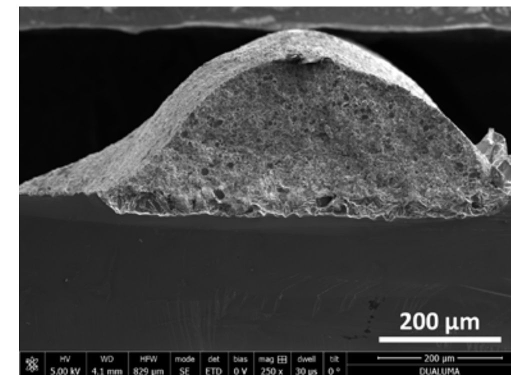

Fig.3. FESEM picture of a cross-section obtained after printing with T1 paste on a textured silicon substrate.

001 Line Speed	Sets the speed of the dispensing head
002 Line Start	Related to the XYZ position to start the line
003 Line Passing	XYZ position in the middle of the line
004 Line End	XYZ position related to the end of the line
005 Step & Repeat Y	Sets the number and the distance between the lines
006 End Program	Step to end the program

Table 1. Program to print lines with a desired distance between them.

Al paste	Mass of wet paste (mg/cm^2)	Mass of dried paste (mg/cm^2)
T1	25.6	20.2
T2	32.6	28.7

Table 2. Specific mass of aluminum paste deposited for the three different pastes.

Al paste	ρ_c (mΩcm^2)	
	Average value	Best value
T1	92	70
T2	54	54

Table 3. Specific contact resistance measured for two aluminum pastes on textured silicon substrates.

Degree of ordering as a function of Sb content in $In_{0.5}Ga_{0.5}P$ layers for tandem solar cells

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1. Introduction

In this work we use Transmission Electron Microscopy for a detailed structural characterization of $Ga_{0.5}In_{0.5}P$ layers grown by metal organic vapor phase epitaxy onto (001) Ge substrates misoriented 6º to [111]. Nowadays, $Ga_{0.5}In_{0.5}P$ is a III-V compound frequently used in multijunction solar cells [1], and developing epitaxial routines that yield highly disordered material is key to attain high efficiency. This alloy might show $CuPt_B$ ordering [2], which consists of an alternation of In and Ga atoms on {111} planes. Although there are four equivalent {111} planes in the zinc-blende structure, order is expected in (-111) and (1-11) planes intersecting the (001) surface along the [110] direction. For GaInP grown on misoriented substrates only one variant prevails, in particular (1-11). A combination of both conventional and aberration corrected microscopy techniques will enable the elucidation of the existing type of ordering and the assessment of the degree of order in the layers as a function of Sb content.

2. Experimental details

The samples, which structure is summarized in table 1, were grown by metalorganic vapor phase epitaxy (MOVPE) using Sb as a surfactant. Different Sb/P molar flow ratios were used in the range 0-3155 ppm.
Samples were thinned up to electron transparency using a Focus Ion Beam (FIB) technique. The samples were prepared in the two orthogonal [110] and [1-10] directions in order to unambiguously establish the type of CuPt ordering. We have used a JEOL 2100 and an aberration corrected Titan FEI operated a 200kV for conventional TEM and high resolution respectively [3].

3. Results

Conventional bright field TEM images, as that shown in figure 1, confirmed the high quality of all epitaxial samples. No evidence of layer decomposition was observed in any case. For cross-section samples along the [110] orientation, the satellite spots observed in selected area diffraction patterns (SAED) at positions (h+1/2,k -1/2,l +1/2) as shown in figure 2, revealed the existence of $CuPt_B$ ordering. Dark field imaging mode using the satellite (1/2,-1/2,1/2) was used to highlight the ordered domains as seen in the bright regions of figure 3, where the dark bands correspond to disordered domains. The domain size as a function of Sb content will be discussed in correlation with the photoluminescence properties.
The samples were also examined with an aberration corrected instrument in scanning transmission electron microscopy high angle annular dark field mode (HAADF) to assess the polarity of III-V dumbbells in the direction of ordering, according to the sensitivity of this mode to the difference in Z number of the constituents present in the sample. In figure 4, an alternation of bright {111} planes at a distance double of d_{111}, clearly reveals the alternation of the indium-rich (Z_{In} = 49, hence more intensity) and gallium-rich planes (Z_{Ga} = 31, hence low intensity) respectively, in good agreement with the presence of satellite spots in SAED. HAADF image at atomic resolution, confirmed the polarity of the semiconductor, with the P atom in the upper position in [110] cross-sections views.
In summary, dark field and STEM-HAADF modes have been applied to assess the type and degree of order in these $Ga_{0.5}In_{0.5}P$ layers. Through this analysis we will be able to correlate MOVPE growth conditions and surfactant action with the microstructure in order to optimize the growth of disordered $Ga_{0.5}In_{0.5}P$ to be used in highly efficient multijunction solar cells.

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[3] The authors acknowledge CCiT from University of Barcelona and LSPMS from École Central de Paris for the use of Microscopy Facilities

Layer	Composition	Thickness(nm)	N(cm3)
Substrate	Ge	150000	1.0·10e18
Nucleation	GaInP	365	
Buffer	GaInP:Sb	1100	≈1.0·10e17
Overbuffer	GaInAs:Si	400	≈8.0·10e17

Table 1 Semiconductor structure of the samples analyzed in this work. All grown layers are fabricated by MOVPE.

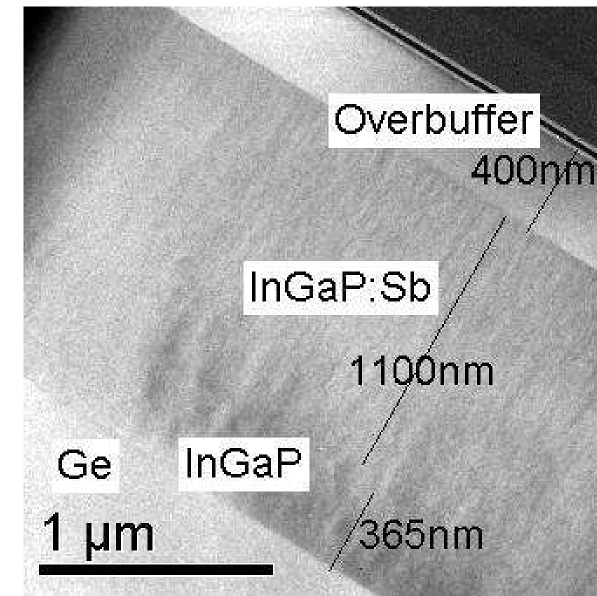

Fig. 1 Bright field image of the whole structure.

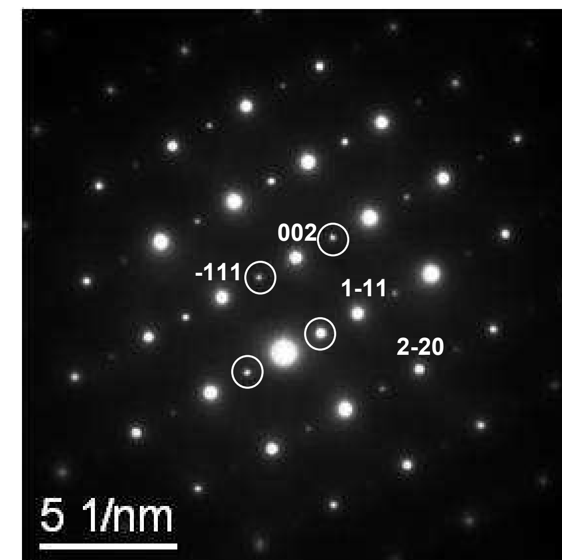

Fig. 2 Experimental diffraction pattern along the [110] zone axis. Notice the superstructure reflections (circles) between the main spots in the direction parallel to g=(1,-1,1)

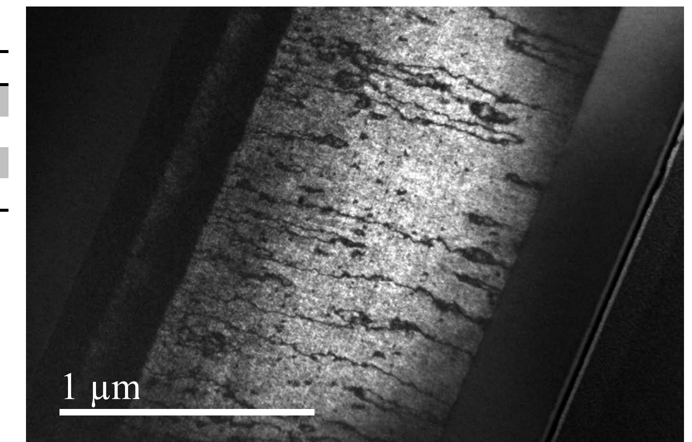

Fig. 3 Dark field image using the {1/2,-1/2,1/2) satellite spot.

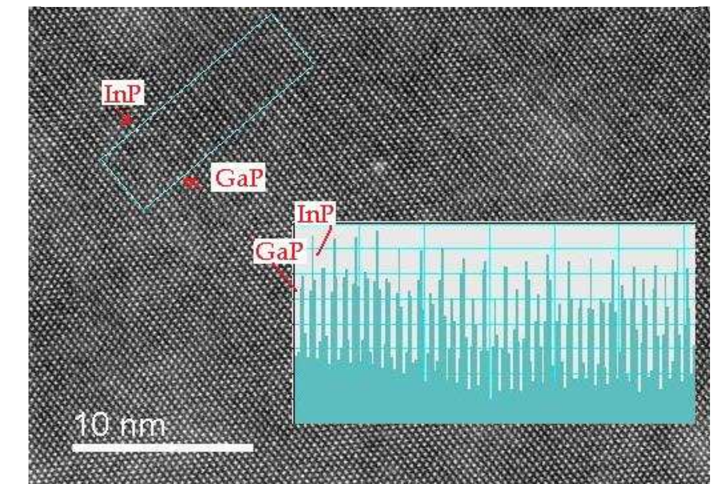

Fig. 4 High Angle Annular Dark Field image (HAADF) in [110] zone axis, showing Ga-rich (darker) and In-rich (brighter) planes along the direction [1-11]. The integrated intensity profile in the squared regions illustrates this double periodicity, since In has a larger Z than Ga.

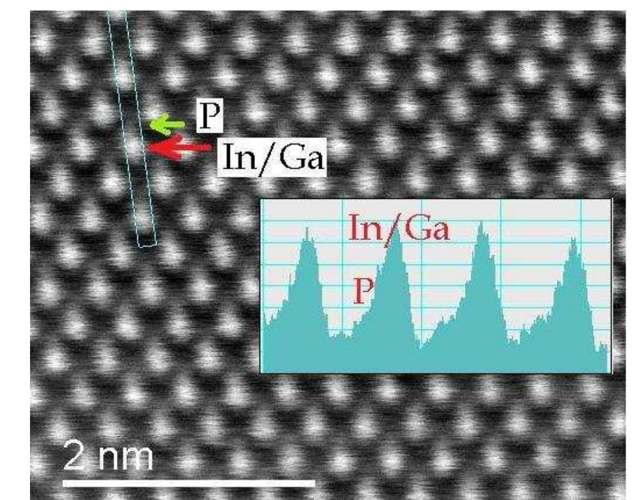

Fig. 5 HAADF image of the dumbbells of GaInP viewed along the [110] zone axis. The element of group V is over the element of group III in this orientation confirming $CuPt_B$ ordering.

Amorphous/crystalline silicon interface characterization by capacitance and conductance measurements

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1. Abstract

Hydrogenated amorphous silicon (a-Si:H) has a great interest for its applications, mainly photovoltaic devices and thin film transistors. Many papers provide different techniques to characterize its properties in order to improve the material quality. A low density of defects at the interface between intrinsic a-Si:H and doped crystalline silicon (c-Si), is crucial for high conversion efficiencies in HIT cells (Heterojunction with intrinsic thin layer).

In this work we have deposited a-Si:H using the ECR-CVD (Electron Cyclotron Resonance Chemical Vapor Deposition) technique, and we have analyzed the a-Si:H/c-Si interface.

In order to obtain the density of defects (D_{it}) of the a-Si:H/c-Si interface, we have followed the conductance method proposed by E. H. Nicollian, normally applied to characterize MIS (Metal-Insulator-Semiconductor) structures [1]. The intrinsic amorphous silicon layer behaves as an insulator for low bias. Values of the D_{it} lower than $10^{11}cm^{-1}eV^{-1}$ were obtained for our devices.

2. Experimental

We have deposited 110 nm of intrinsic a-Si:H on n-type <100> crystalline silicon (c-Si) wafers with a resistivity ρ= 1-10 Ωcm using the ECR-CVD technique with an Astex-4500 reactor. The substrates were cleaned by a standard RCA process, followed by a dip in diluted HF. This last step was performed in nitrogen atmosphere, right before loading the substrates into the deposition chamber, without exposing them to air. For electrical characterization, metal electrodes (100 nm Ti + 200 nm Al) were deposited by e-beam evaporation. Devices with different area ($3.97·10^{-3}cm^2$, $2.5·10^{-3}cm^2$, $9·10^{-4}cm^2$ and $4·10^{-4}cm^2$) were defined by optical lithography

Capacitance and conductance measurements as a function of applied voltage were performed using an Agilent 4294A impedance analyzer at frequencies from 1 kHz to 1MHz. I-V characteristic were obtained with a Keithley 2636A SMU (Source Measure Unit) from -6V to 2 V. With these measurements, we can apply the method described in ref. [1], considering that the intrinsic a-Si:H layer behaves as an insulator. Therefore, the Dit at the interface between c-Si and a-Si:H is obtained.

FTIR (Fourier Transform Infrared Spectroscopy) characterization has been performed in a Nicolet Magna-IR 752 spectrometer, in a wavenumber range from 340 cm^{-1} to 4000 cm^{-1}. This technique allows to determine the bonding structure of the films, and the hydrogen content from the Si-H related absorption bands.

3. Results and discussion

In Fig. 1 we present the conductance measurements as a function of bias voltage for different frequencies. We observe the same behavior expected for MIS structures with a clear maximum located at -1 V, that we attribute to the influence of interface traps. The increased conductance observed for positive voltage is related to series resistance. Figure 2 shows the capacitance-voltage measurements The shape of the curves seems to indicate that in our structures the accumulation region is achieved, allowing to compute the capacitance of the a-Si:H layer and the series resistance, which are required to obtain the D_{it}.

Table 1 shows the Dit values for our devices. These values for the a-Si:H / c-Si interface are lower than those reported for a-Si:H deposited by CVD, (around $5·10^{11}cm^{-1}eV^{-1}$ [3]). This result indicates a high quality a-Si:H/c-Si interface.

The FTIR spectra present only the Si-H related bands at 640 cm^{-1}, 2090 cm^{-1} and 850 cm^{-1} [2] that confirms the high purity of the films.

4. Conclusions

In this work we have demonstrated the applicability of the conductance method to characterize a-Si:H/c-Si structures. Values of the Dit as low as 10^{11} cm^{-2} eV^{-1} have been measured for a-Si:H deposited by ECR-CVD .

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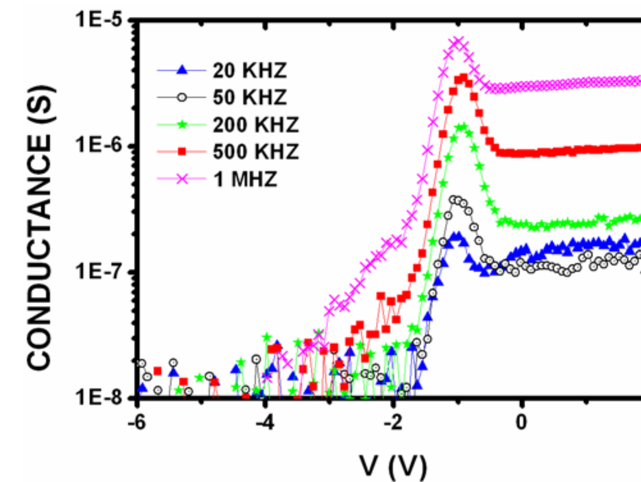

Fig. 1 Conductance measurement for different frequencies for $9·10^{-4}cm^2$ sample. We can observe a maximum in the graph due to the effect of the interface traps.

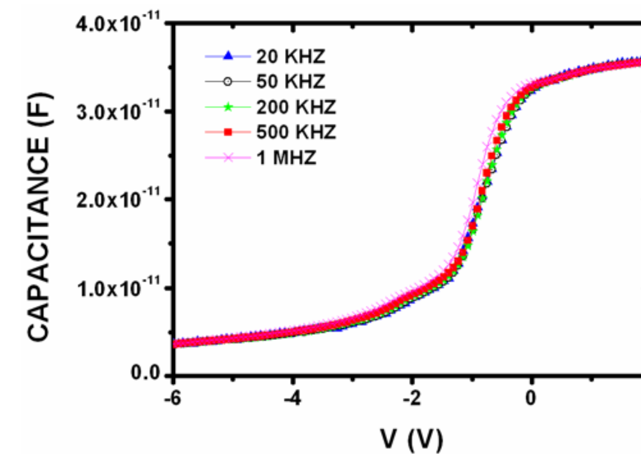

Fig. 2 Capacitance measurement for different frequencies. The same shape than in MOS structures is observed, with accumulation region.

Area (cm^2)	$2·10^{-3}$	$9·10^{-4}$	$4·10^{-4}$
D_{it} ($cm^{-1}eV^{-1}$)	$9·10^{10}$	$8·10^{10}$	$8·10^{10}$

Table 1. Dit for different sample size. We obtain almost the same value for the three.

A tool to deploy nanodevide simulations on Cloud

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1. Abstract

The emerging of cloud computing has made it possible to deploy scientific applications in which users can manage the computational capacity on demand. In order to provide for the nanodevice researches the flexibility they require, we present in this paper the Flexible Cluster Manager (FCM). We have developed this tool to deploy Sentaurus TCAD virtual clusters on demand on cloud infrastructures, by means of a web interface. It is also possible to use it with other commercial or in-house simulator tools.

2. Introduction

Historically, cluster computing has played an important role in the support of the high demanding computation of the scientific simulations. Nowadays, with the emerging of the clouds as the 5th utility [1], it is possible to adapt on demand the computing capacity to the requisites of users, allowing them to increase or reduce the computational resources according to their needs. Usually, the research centers own computer clusters. However, in most cases the clusters are shared by the different research groups in these organizations that can even have incompatible software requirements. In order to overcome this situation and provide the flexibility necessary in the management of the computational resources, we have developed the Flexible Cluster Manager (FCM). It allows us to automatically deploy Sentaurus [2] virtual clusters on demand on cloud infrastructures by means of a web interface.

3. Sentaurus on FCM

Sentaurus is a suite of TCAD tools that can simulate the manufacturing and the operation of semiconductor devices, including silicon and compound semiconductor technologies. Sentaurus TCAD suite includes support for process simulations, structure editing and device and interconnect simulations. It also provides frameworks such as Sentaurus Workbench, Sentaurus Visual and Sentaurus PCM Studio.

Flexible Cluster Manager (FCM), the tool we have developed, allows deploying Virtual Clusters (VC) on demand under a cloud infrastructure. FCM is able to deploy VCs without user intervention at all, instantiating the required Virtual Machines (VMs) and configuring automatically the service the user selects, including Sentaurus TCAD. FCM is able to modify the cluster size online without interfering with the on-going cluster operations, allowing the users to add additional nodes or to remove the unnecessary ones. The workflow to deploy Sentaurus by means of FCM is depicted in Fig. 1. The user employs a web client to access the FCM web interface. It is required to provide the data necessary to deploy the VC, such as the cloud provider, the OS template, the service offering, the software package (Sentaurus TCAD) and the cluster size (number of nodes). FCM will automatically deploy the Storage VM in which the Sentaurus workspace will be allocated, the Head VM that is intended as the front-end, in which Sentaurus workbench can be accessed; and the Node Vms, which are intended as the elements that provide the computing capacity. The FCM deployment time of virtual clusters, employing commodity hardware, is depicted in Fig. 2. It includes the deployment time of the VMs (VM Deploy), the time required to create a bare cluster (Basic Package) and the time to deploy Sentaurus (Sentaurus TCAD). The cloud infrastructure employed is based on Apache CloudStack 4 [3], an open-source cloud management that allows deploying private, public and hybrid clouds under the Infrastructure as a Service model. It employs KVM as the managed hypervisor, and the VMs are deployed in computer nodes that have Intel Core i7-2600@3.40 GHz processors and CentOS 6.3 64 bit as OS. The interconnection network is Gigabit Ethernet.

4. Conclusions

Flexible Cluster Manager allows deploying automatically Sentaurus virtual cluster on demand by means of a web interface. It provides important advantages, allowing scaling the computational resources to perform simulations elastically as they are required. Notice that the unused computer resources could be employed to perform other tasks, increasing the reuse ratio of these resources.

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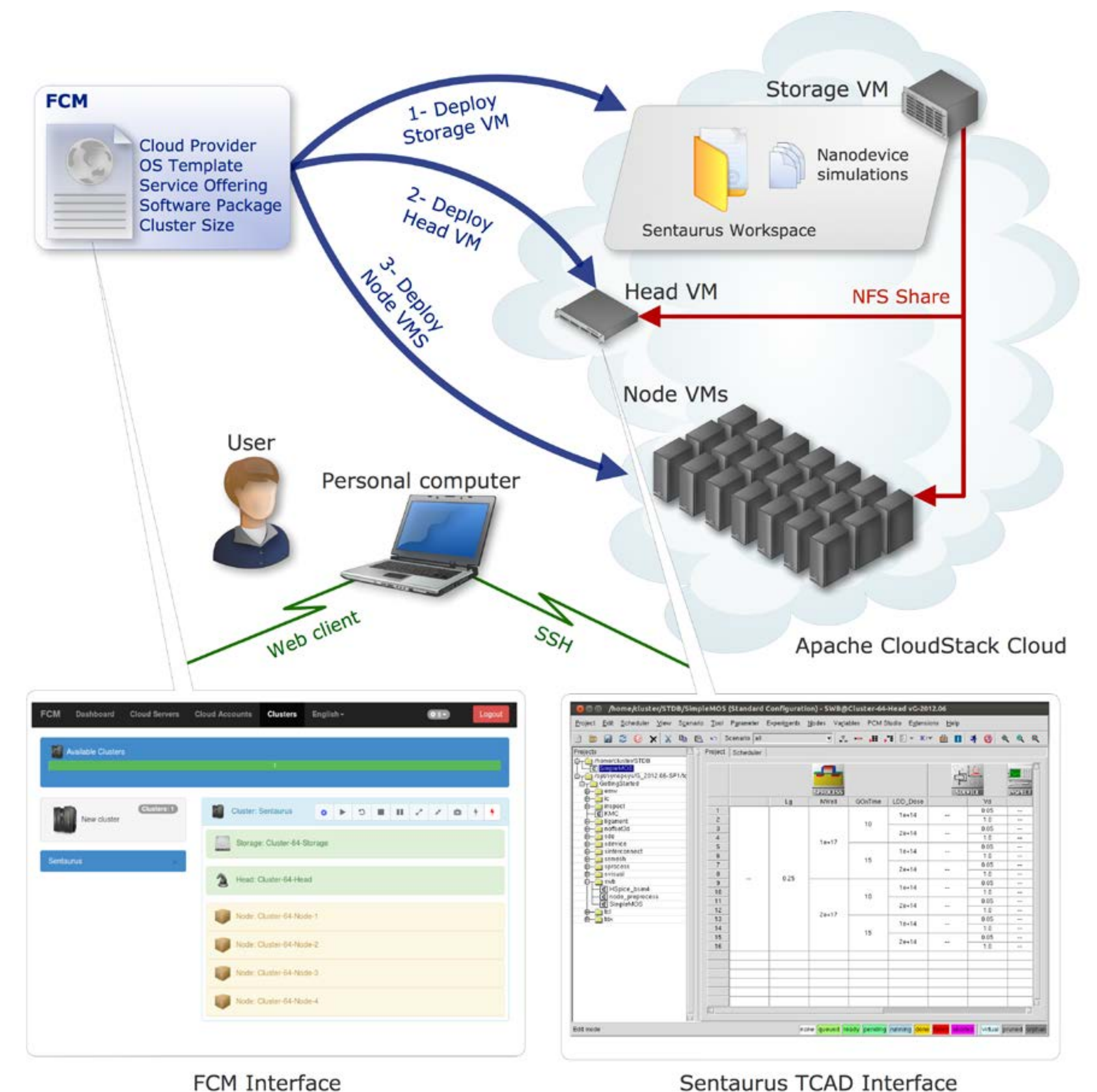

Fig. 1. Workflow to deploy Sentaurus TCAD by means of FCM

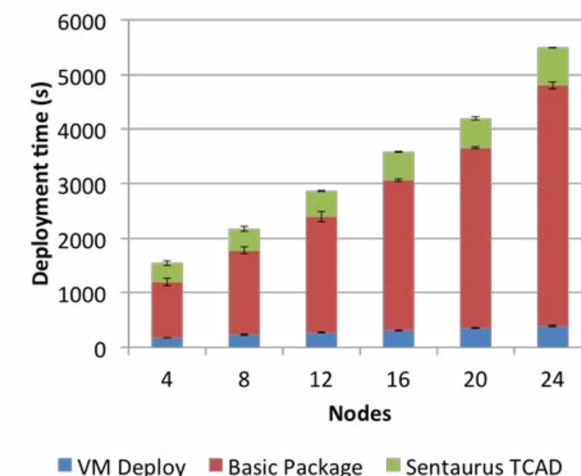

Fig. 2 Deployment time of Sentaurus TCAD Virtual Clusters

ZnO conductometric sensor for indoor air quality measurement inside buildings

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1. Abstract

The objective of this work is to develop a ZnO conductometric gas sensor to monitor two key pollutants in indoor environments: benzene and formaldehyde. Conductometric sensors are widely used for this purpose [1,2] The final aim of the sensor is to be integrated in an air quality measuring system connected to the HVAC (Heat Ventilation and Air Conditioning) system so ventilation is activated according to the air quality within the building. As there is no EU common legislation about the target gases and detection limits, the authors have set them according to the recommendations of different agencies in Europe and the US.

2. Introduction

Volatile Organic Compounds (VOCs) can contribute to poor Indoor Air Quality (IAQ). Benzene and formaldehyde are two VOCs found among the five indoor-originated compounds considered the most hazardous, according to the results of the INDEX EU project [3]. Both formaldehyde and benzene have been classified as a human carcinogen and are dangerous at very low concentrations. The OSHA (Occupational Safety & Health Administration) states a STEL (Short Term Exposure Limit) of 5 ppm and an action level of 500 ppb for benzene, while the STEL for formaldehyde is 100 ppb and action level is 500 ppb.

3. Experimental

The sensing devices are conductometric sensors fabricated on 0.5 mm-thick alumina substrates. Chips are squares of 2.5 mm x 2.5 mm (Figure 1). The heater and the sensing element are on the same side of the chip and the sensing area is 0.5mm x 0.5 mm over the. The heater and the interdigitated electrodes were fabricated using a 200 nm-thick platinum obtained by DC sputtering shaped by lift-off. As a second step, the Vapour Solid (VS) technique [4] was used to grow ZnO nanostructures in situ over the Pt electrodes. The fabrication steps are shown in Figure 2. Two packaging options were tried: suspended and glued to the TO holder and then the power consumption of the sensor was characterized through a thermography infrared camera. The characterization of the sensors' signal was performed inside sealed chambers using a mixing system consisting of mass flow controllers (MFCs) and an automated data acquisition system controlled by a PC.

4. Results and discussion

The experiments about power consumption show that the glued sensor requires three times more power than the suspended one (Figure 3). At a working temperature of 250ºC, the suspended sensor requires 0.4 W, while the glued sensor needs 1.2 W. Despite of the higher consumption, the glued sensor is more robust for handling. The sensing area is held at uniform temperature with the designed heater.
The ZnO sensor response to the target VOCs was also measured in a controlled atmosphere of benzene in air or formaldehyde in air. The response is calculated as the resistance change ratio (in percentage). This ratio is positive for n type (such as ZnO) semiconducting oxides and reducing gases (such as benzene and formaldehyde). Figures 4 and 5 show a sequence of decreasing pulses of 30 minutes of the VOC concentrations followed by 30 minutes in clean air. The ranges go down to 500 ppb in the case of benzene (Figure 4) and down to 50 ppb in the case of formaldehyde (Figure 5). The sensor shows a good recovery of the baseline and the time of (t_{90}) is 1.5 min for 10 ppm of benzene and 1 min for 10 ppm of formaldehyde.

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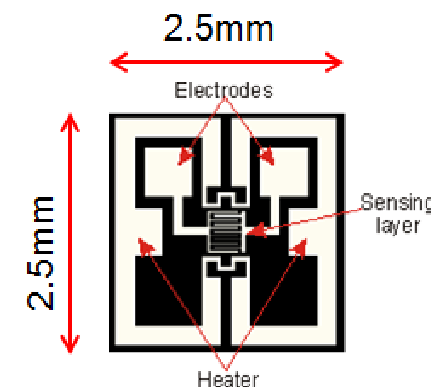

Figure 1. Sensor layout

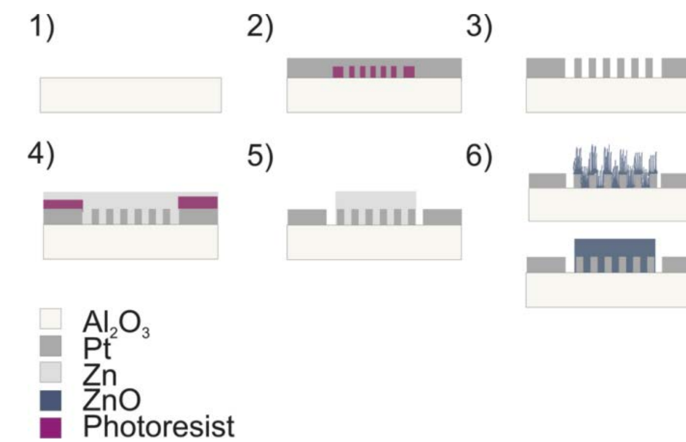

Figure 2. Steps for sensor fabrication

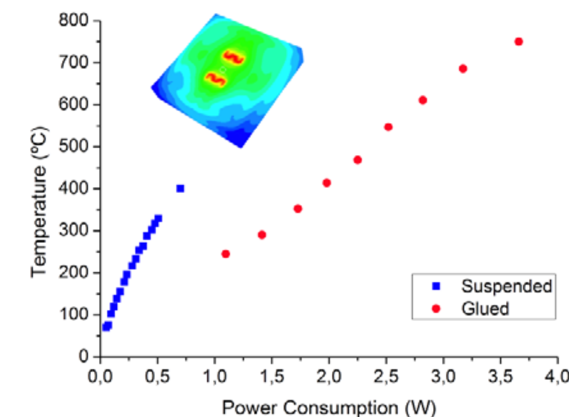

Figure 3. Power consumption of the glued and suspended sensor and simulation of the temperature distribution

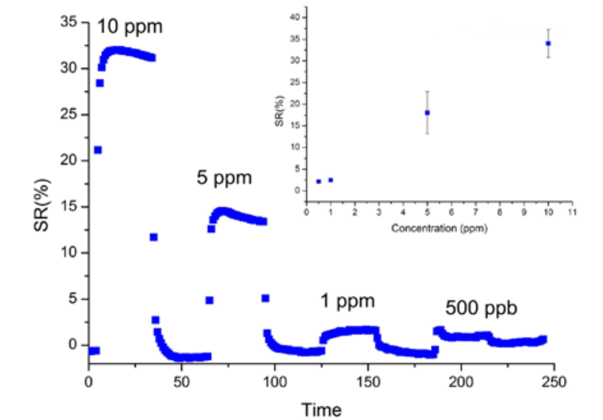

Figure 4. ZnO sensor response to benzene concentrations from 10 ppm to 500 ppb and sensitivity plot (inset) at 250ºC and no humidity

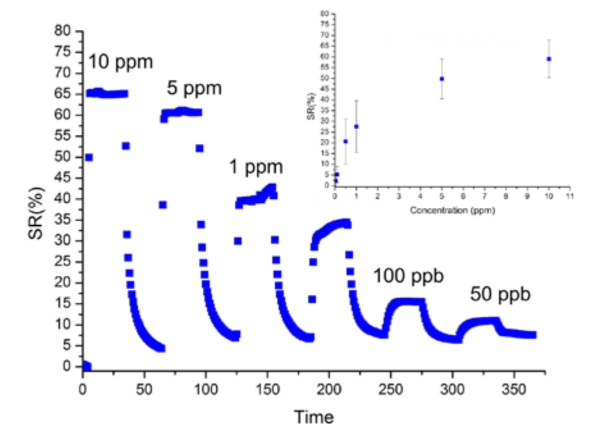

Figure 5. ZnO sensor response to formaldehyde concentrations from 10 ppm to 50 ppb and sensitivity plot (inset) at 250ºC and no humidity

Graphene devices fabricated by laser

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Abstract

Graphene, has attracted increasing attention in recent years [1] due to its excellent mechanical, optical and electrical properties. Its high theoretical surface area (2630 m2 g-1) and high electrical conductivity make it an attractive material for many industrial applications [2]. Also is a flexible transparent material that can be used for solar cells, light emitting diodes (LEDs, OLEDs), touchscreens and LCD displays [3].And in the near future, its flexibility will let to create foldable and wearable devices [4].

A layer of graphene can be prepared by several techniques: by mechanical exfoliation from graphite, by precipitation on a silicon carbide surface, or by chemical vapor deposition growth on Cu or Ni. All these techniques produced high quality graphene but are quite expensive for industrial applications. In the other hand, the reduction of graphene oxide (GO) is an alternative low cost technique for having graphene material.

In our case, the reduction of the GO was achieved by using a DVD laser. This is a single-step and scalable procedure which allows to make circuits and complex designs on different substrates without the need for chemicals, masks, transfer techniques, catalysts or expensive equipment [5, 6]. Furthermore, by varying the laser intensity and the number of times that GO is exposed, we can control the reduction degree of the oxide and, consequently, its electrical properties.

The material obtained by this reduction process proves to be mechanically robust with a high electrical conductivity and a high specific surface area, suggesting that this laser reduced graphene (LRG) may be used for manufacturing electronic devices or chemical sensors [7].

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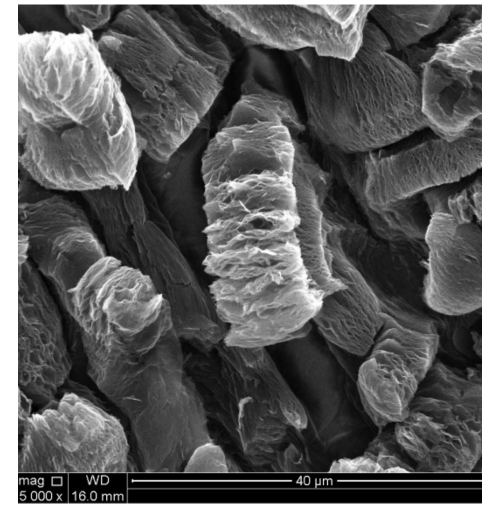

Fig. 1. SEM picture of the reduced graphene oxide by laser.

Use of an electronic nose as a tool to differentiate winemaking techniques

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1. Abstract

This paper reports a novel application of a portable and wireless sensor system (e-nose) to differentiate, through recognition and detection of different white grape variety types, different winemaking techniques. This portable system is a fast tool that can differentiate between elaboration methods: conventional or cold maceration. In addition both methods have been treated with yeasts on lees, "lees", and finally they have been compared with those ones without yeasts, "no lees".

2. Introduction

The actual interest in improving and promoting the quality of wines has opened new searching lines [1, 2].
The use of a portable sensor system, that allows the discrimination of different varieties and a correct varietal classification of samples subjected to different modes of elaboration, could be used in the future as a new tool to differentiate winemaking techniques.
In this work, two types of winemaking have been made in white wines: conventional and prefermentative cold maceration. Once racked wines, an aliquot of each preparation was taken and treated with yeast extracts for treatment on lees (lees), for four months. Thus, it has been possible to compare, for each variety, this treatment with the usual (no lees) after the fermentation has been completed. This treatment is intended to make wines of greater olfactory and gustatory complexity. However, from the olfactory point of view, the treatment with yeasts on lees, sometimes, confers a degree of uniformity in the aroma profile, which does that the originated subtle changes are not always detected. Therefore it would be good to have an analytical tool (electronic nose) in order to assist to the winemaker on: first, to discern the elaboration method of the wines and if they have been treated with yeasts on lees, and second, to have an index of the correct course of treatment.

3. Experimental

In this work, a portable e-nose (WiNOSE 2.0), designed in our laboratory, has been used to measure elaborated wine samples with different techniques, using four white grape varieties: Malvar (MAL), Malvasia(MVS), Viognier (VG) and Chenin Blanc (CHB).
The measurement system is composed by: (1) Volatile organic compounds extraction method. (2) Peltier cooler. (3) WiNOSE 2.0 with a resistive sensor array over micromechanized silicon hot plates. (4) Control system. In Fig. 1 a scheme of the total measurement system is shown.

3. Results

We have analyzed the measurements realized by the e-nose for the four white grape varieties subjected to the different methods of elaboration already cited: Conventional "with lees" and "without lees" and cold maceration "with lees" and "without lees", by Principal Component Analysis (PCA). In Fig. 2, it is shown the discrimination between Malvasia samples subjected to the conventional method "with lees" and "without lees", observing a good differentiation. The same happened for the case in which Malvasia samples were subjected to the maceration method (Fig. 3). In Fig. 4 and Fig. 5, it is observed that the two methods of elaboration are also well separated for the Malvasia variety with lees and without lees, respectively. This fact happened, in general, for each variety. The e-nose has also been able to perform a good separation among the studied varieties for the elaboration methods. Fig. 6 shows a clear discrimination for the four varieties prepared with the conventional method and treated with yeast extracts.

4. Conclusions

A novel and complex application in the wine has been possible to carry out through a portable e-nose, that allows the differentiation of different varieties and the varietal correct classification of samples subjected to different modes of winemaking.

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Fig. 1 Measurement set-up

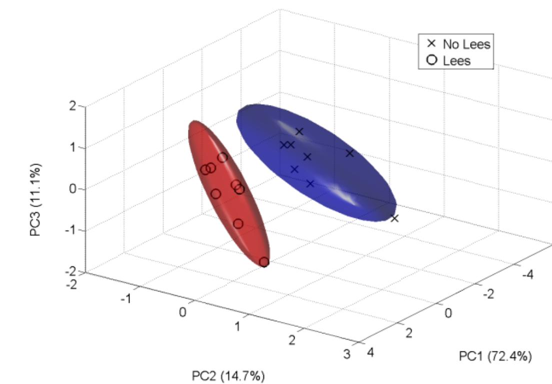

Fig. 2 PCA plot for Malvasia samples subjected to the conventional method "with lees" and "without lees"

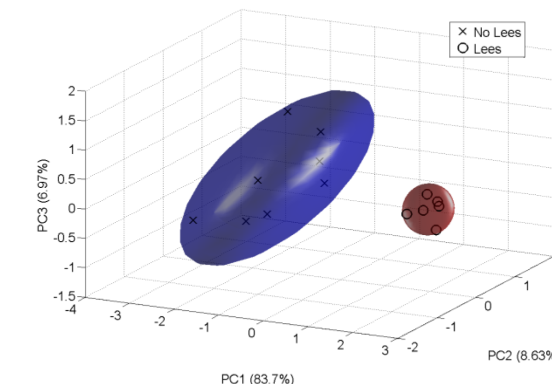

Fig. 3 PCA plot for Malvasia samples subjected to the maceration method "with lees" and "without lees"

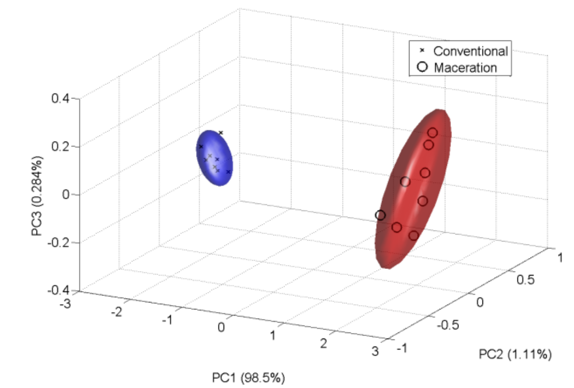

Fig. 4 PCA plot for Malvasia samples subjected to the conventional and maceration methods with lees

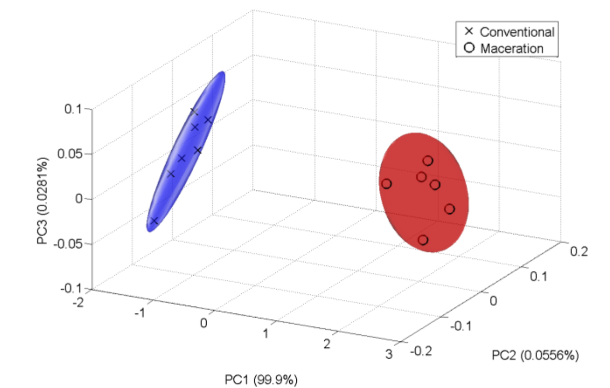

Fig. 5 PCA plot for Malvasia samples subjected to the conventional and maceration methods without lees

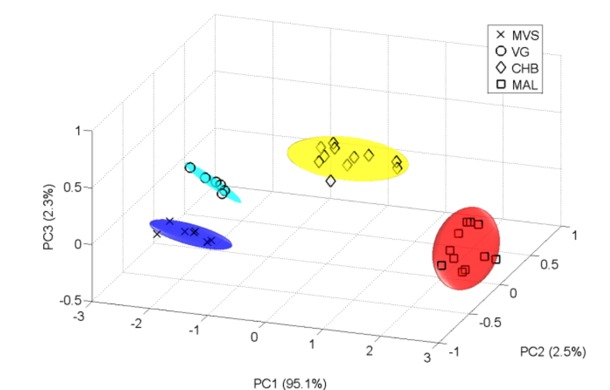

Fig. 6 PCA plot for the samples of four white varieties subjected to the conventional method with yeast extracts on lees

Optoelectronic properties of small defect clusters in Si from multiscale simulations

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1. Abstract

We have performed a multiscale simulation study for evaluating the optoelectronic properties of small defect clusters in Si. We used Molecular Dynamics (MD) simulations for finding relevant defect configurations, and *ab initio* simulations for elucidating their optoelectronic properties.

2. Introduction

Defects in crystalline Si (c-Si) introduce electronic states in the gap, which can modify the carrier recombination pathways. In particular, the photoluminescence (PL) spectra of c-Si shows radiative recombination pathways associated to defects [1]. Thus, PL could be used as a non-destructive technique for defect identification [2]. Nevertheless, not all defects responsible for PL lines in c-Si have been identified. For example, the W and X PL lines, with photon energies of 1018 meV and 1039 meV respectively, are generated during ion implantation and annealing and are associated to small interstitial defect clusters [1, 3]. Different defect configurations have been proposed for these PL centers, and analyzed using *ab initio* simulations [4, 5]. These studies revealed contradictory results, and the configuration of the W and X centers is not clear yet. In addition, X and W PL lines have gained great interest in Si photonics [6]. The knowledge of the defects responsible for the X and W PL lines can help to optimize the fabrication processes of devices to enhance their presence. Here we propose a systematic procedure for identifying defects that can be responsible of W and X PL lines in c-Si.

3. Simulation details

We used MD simulations of implantation recoils and annealings to obtain defect configurations from atom dynamics, rather than presupposing configurations as it was done in previous works [4, 5]. These simulations emulate the processes that result in the small interstitial defects responsible for the W and X PL lines. We used *ab initio* simulations to calculate the band structure and the electronic density of states (EDOS) of found defects.

4. Simulation results and discussion

In this work we followed this procedure:

1. We obtained a large set of defect configurations from our MD simulations. We considered those with the known experimental symmetry of W and X centers [1]. We show in Fig. 1 some of the obtained defects on convenient orientations to highlight their symmetry. Tri- and tetra-interstitial defects shown were studied previously [4, 5]. I_3-a and I_4 defects were proposed by Ref. 5 as W and X centers, respectively; while Ref. 4 could not corroborate it.
2. We evaluated the band structure and EDOS for each defect, as it is shown in Fig. 2 for the I_2 defect of Fig. 1. This defect introduces two bands in the gap (labeled as 1 and 2), and another band on top of the valence band (VB) (labeled as 3). Mid-gap bands are expected to result in non-radiative recombinations. Remaining defects of Fig. 1 introduce bands at the top of the VB or close to it (not shown), which make them good candidates to PL centers.
3. For these candidates to PL centers, we evaluated the occupation probabilities relative to band edges for carrier transitions between bands at 300K, which are shown in Fig. 3. There is a significant increment at the X point for the I_3-b defect, and at the Γ point for the I_3-c. This increment is necessary for radiative carrier recombinations.
4. We also calculated the energy difference between the defect level and E_v ($E(0/+) – E_v$) as it was done in Ref. 5. Obtained values are shown in Table 1, along with experimental data (from Ref. 5 and references therein). There is a good agreement for the I_3-b defect with the W line, but none of the candidates for the X center agree with experimental data.

To summarize, promising new evidences were found for the W center, while our results do not support the configuration previously proposed as X center. We continue searching for defect configurations suitable for W and X centers in c-Si, and performing *ab initio* calculations for validating our findings.

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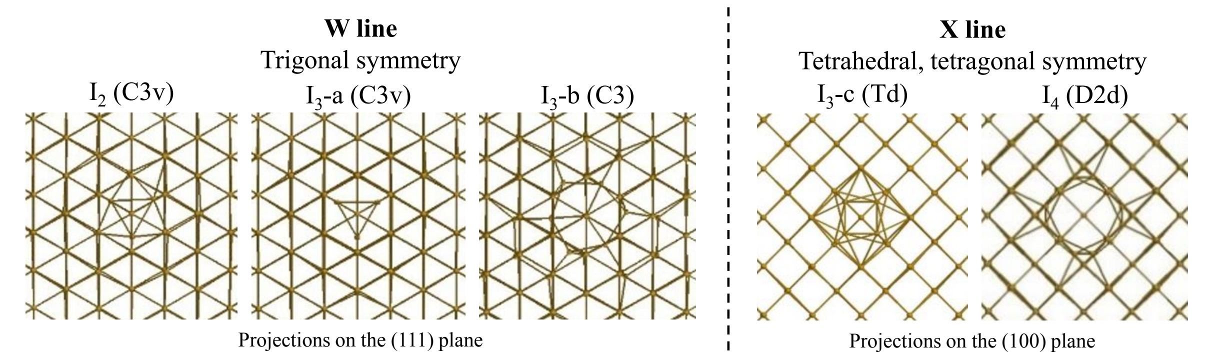

Fig.1. Snapshots of some of the defects considered. Defect configurations are projected on the appropriate plane for visualizing their symmetry. The defect nature (di-, tri-, tetra-interstitial) and its symmetry are written over the snapshots.

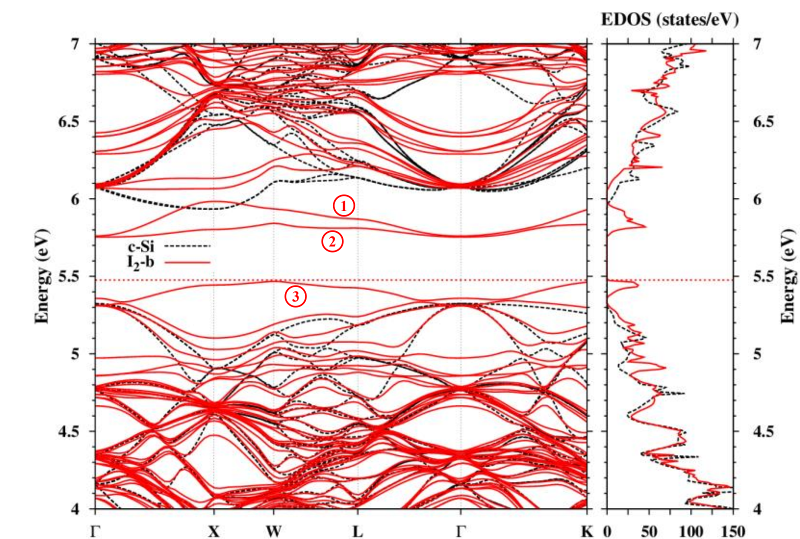

Fig.2. (left) Band structure and (right) EDOS for the I_2 defect of Fig. 1, and for c-Si. Horizontal red dashed line shows the position of the Fermi level for the I_2 defect. Numbers are used to label bands in the gap region (see text for details)

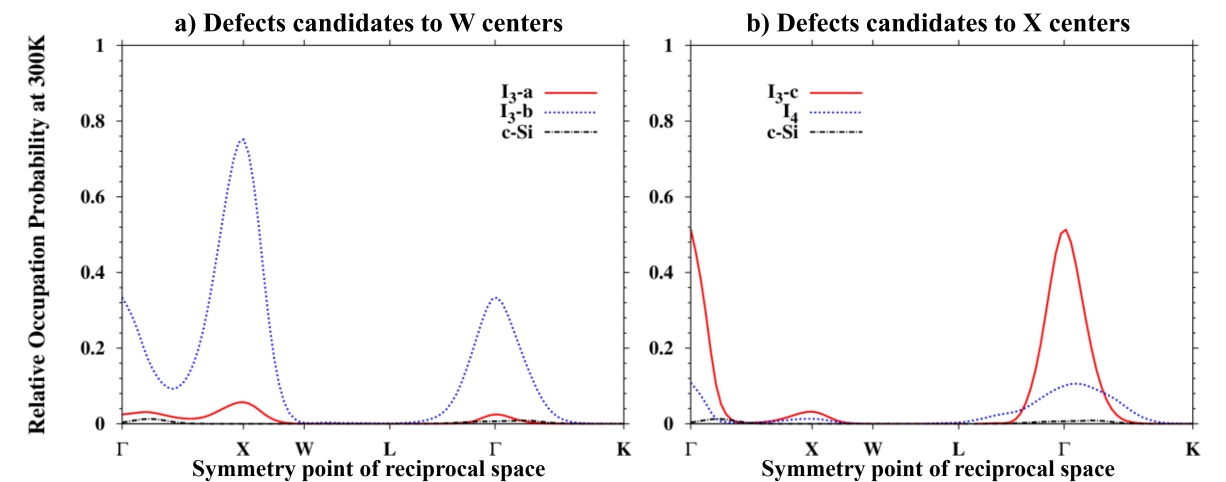

Fig.3. Occupation probabilities relative to band edges for carrier transitions between bands at 300K from electronic energies of band structure calculations.

Defect	E(0/+) - E_v (eV)
I_3-a	0.125
I_3-b	0.152

Defect	E(0/+) - E_v (eV)
I_3-c	0.059
I_4	0.248

Table 1. Energy difference between the defect levels and E_v. Experimental values are 0.15 eV for the W line, and 0.13 eV for the X line (from Ref. 5 and references therein).

Evaluation of the Thermal Resistance in GaN-Diodes by means of Electro-Thermal Monte Carlo Simulations

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1. Abstract

An electro-thermal method coupled with an ensemble Monte Carlo (MC) simulator is employed to extract the value of the thermal resistance, R_{th}, in an un-gated $Al_{0.27}Ga_{0.73}N/GaN$ heterostructure. Different substrates (polycrystalline diamond - PCD, diamond, Si and sapphire), and die dimensions will be analyzed.

2. Introduction and Modeling Approach

In spite of the strong potentiality of GaN and AlGaN/GaN based devices for high-power and high-frequency applications, their utilization is limited by the elevated lattice temperatures reached inside them, being this excessive overheating the main hindrance to their reliability and use [1]. Therefore, the correct description of self-heating effects is essential for the accurate modelling of GaN-based devices. For this purpose, we have expanded the capabilities of our home-made, semi-classical Monte Carlo (MC) simulator, proved to be a very efficient tool to investigate electron transport and optimize the static, dynamic and noise operation of semiconductor devices [2]-[3], to a full electro-thermal model. Specifically, we have coupled our MC simulator with the solution of the steady-state heat diffusion equation (HDE) [4]-[5]. Note that a sufficient number of iterations of the HDE-MC solver must be carried out in order to reach a convergence of the static electro-thermal solution.

The geometry of the $Al_{0.27}Ga_{0.73}N/GaN$ diode under analysis is shown in Fig.1. The distance between the contacts is 2 µm. The electronic and thermal simulations take place in two different domains, also sketched in Fig. 1. Piezoelectric scattering and those with phonons and dislocations are included in the model. To correctly simulate the heterolayer we incorporate the influence of spontaneous and piezoelectric surface polarization charges: P=12.12×10^{12} cm^{-2}. In addition, a surface charge density σ = - 4.12×10^{12} cm^{-2} is placed at the top of the AlGaN layer, which appears as a result of polarization charges partially compensated by charge trapped in surface states. A Dirichlet boundary condition for the HDE is imposed at the bottom of the structure (a heat sink with a constant temperature T_h). At 300 K, we consider the following temperature-independent thermal conductivities, k=30, 130 and 300 W/(K·m) for AlGaN, GaN and Au, respectively.

Models using a thermal resistance, where the lattice temperature inside the device, T_{latt}, is updated according to the formula $T_{latt}=T_h+P_{diss}\times R_{th}$ (being P_{diss} the dissipated power) are currently applied to evaluate the thermal behaviour of devices due to their simplicity and lower time consumption with respect to another algorithms. However, in this approximation the value of R_{th} is usually extracted phenomenologically. As an interesting alternative, the HDE-MC simulator allows us to extract the value of this thermal resistance, and also in some cases, obtain its dependence on the geometry and thermal parameters of the device.

2. Results and Discussion

We examined through the HDE-MC simulator the effect of varying (1) the thermal conductivity of the substrate (k_s), and (2) the semiconductor die dimensions (L_1, L_2). In Fig. 2 and Fig. 3 we show the *I-V* curves and the average temperature in the electronic domain (T_{av}) *vs.* dissipated power, respectively, for devices grown on different substrates. HDE-MC simulations allow us to calculate R_{th} by fitting the T_{av} dependence *vs.* dissipated power. As expected, the substrate asserts a strong influence over the self-heating of the device. In Fig. 4 we have represented the profiles of the increase of lattice temperature for a bias of 6 V at three different *y*-positions (channel, interface MC-HDE domains and interface buffer-substrate). The sapphire material causes an enormous temperature rise.

In Fig. 5 we analyse the dependence on R_{th} respect to die dimensions L_1 (bottom axis) and L_2 (top axis). When L_1 increases above 250 µm, R_{th} remains almost constant, 13.3 K·mm/W. As L_2 is reduced, the thermal resistance is lower as expected, and therefore better heat dissipation is obtained. We predict values of R_{th} in the range between 10-20 K·mm/W in both cases.

Preliminary results indicate that for a temperature-dependent conductivity, the relation between T_{av} and P_{diss} is not linear. In this case R_{th} is function not only of the geometry and materials of the die, but also of the dissipated power. All these results will be shown and described in detail at the conference.

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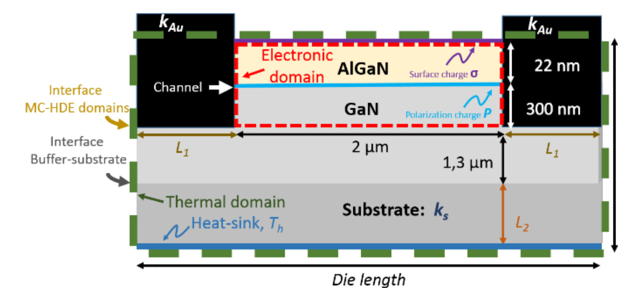

Fig. 1. Schematic structure of the un-gated $Al_{0.27}Ga_{0.73}N/GaN$ diode under study.

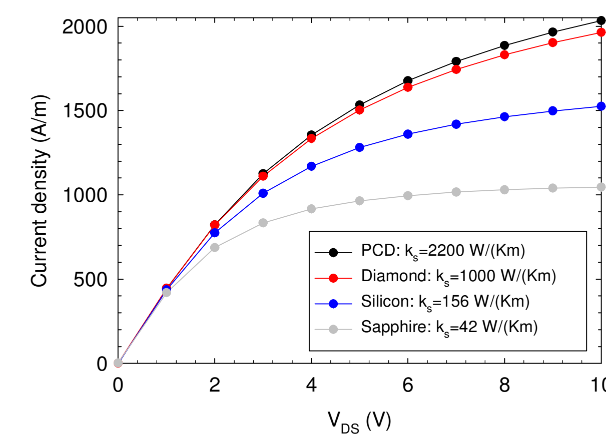

Fig. 2. *I-V* curves for different substrates: PCD [k_s=2200 W/(K·m)], diamond [k_s=1000 W/(K·m)], silicon [k_s=156 W/(K·m)] and sapphire [k_s=42 W/(K·m)]. L_1=200 µm and L_2=300 µm.

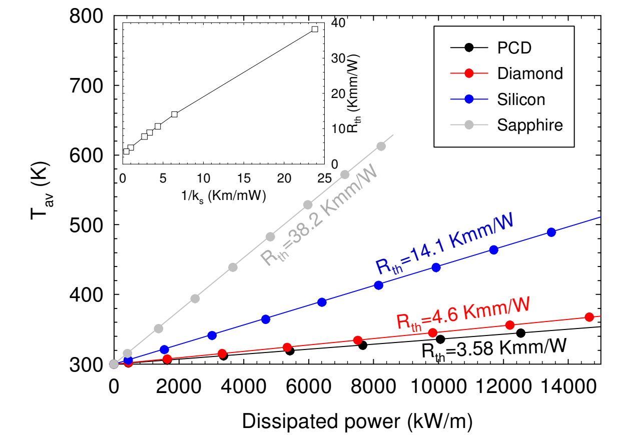

Fig. 3. Analysis to evaluate the influence of k_s in the simulations. Average temperature, T_{av}, *vs.* dissipated power and linear fitting to extract the corresponding thermal resistance. The inset shows R_{th} *vs.* 1/k_s. L_1=200 µm and L_2=300 µm.

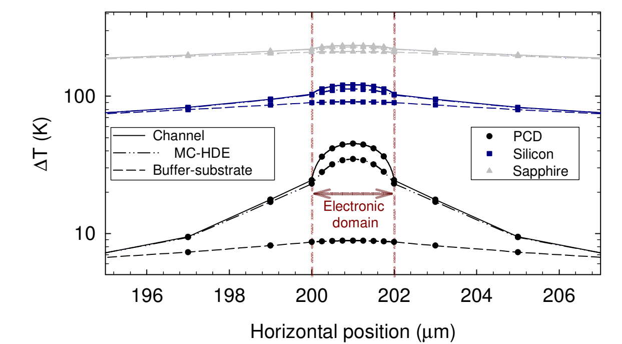

Fig. 4. Profile of the increase of lattice temperature (ΔT=T_{latt}-T_h) for three different *y*-positions (channel, interface MC-HDE domains and interface buffer-substrate, see Fig. 1) for a bias of 6 V.

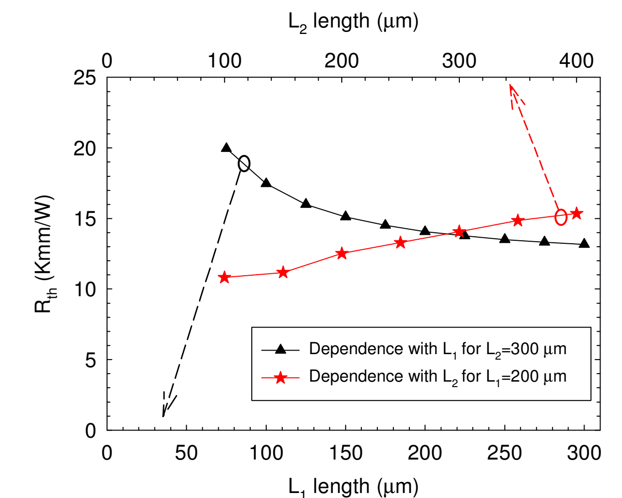

Fig. 5. R_{th} *vs.* die dimensions (a) L_1 (bottom axis, L_2=300 µm) and (b) L_2 (top axis, L_1=200 µm). Both cases are for k_s=156 W/(K·m).

Modeling of nanocalorimetry experiments to investigate the kinetics of damage annealing in self-implanted Si

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1. Abstract

We have performed non-lattice Kinetic Monte Carlo (KMC) simulations to study the heat released by annealing ion implanted damage in silicon. The model try to identify the atomistic mechanisms responsible for nanocalorimetry signals in self-implanted silicon.

2. Introduction

Nanocalorimetry is a thin-film equivalent of Differential Scanning Calorimetry (DSC) that allow measure the heat associated with transformation or reactions occurring in layers of the order of a few monolayers [1]. The scanning rate, 10^5 K/s, and the low thermal losses make this technique orders of magnitude more sensitive to near-surface thermal processes. It is thus a valuable tool to investigate *in situ* the kinetics of damage annealing [2]. But this process is complex and it is difficult to distinguish all the mechanisms and energetics involved. The goal of this work is to develop a model that reproduces ion implanted Si nanocalorimetry experiments and to assign specific experimental signals to different stages of defect evolution.

3. Model

In this work, we use a non-lattice KMC atomistic model of defect generation and annealing to follow the evolution of ion beam induced defects at sizes, time and temperatures scales of experiments. Along with Si self-interstitials and vacancies and their clusters, the model also consider the bond defect. In this model, the amorphous regions are considered as agglomerates bond defects [3]. This defect can be formed during the collision cascade and when a self-interstitials and a vacancy interact, before complete recombination. It is characterized by a formation energy and a recombination barrier whose values depend on the number of neighbouring bond defects. This model simplifies the complex atomic relaxation scenario by reducing the number of possible configurations to a small finite set, but it reproduces the main processes of experimental nanocalorimetry scans under different implant conditions.

4. Results

We present in Fig.1 some simulation results and the comparison with experiments by Anahory [4]. Figure 1 corresponds to samples implanted at room temperature with 10 keV Si ions with different doses followed by a temperature ramp-up at a rate of 10^5 K/s. We observe that the signal amplitude increases with dose until it saturates. At higher doses, there is a uniform heat release from 500 to 900 K and then a peak appears at ~1100K. At low doses, most defects recombine quickly so that the signal extinguishes as temperature increases. The uniform heat release is attributed to the structural relaxation of the amorphous layer [5]. In our model, we can correlate these curves by with defect evolution. Figure 2 is an example that shows the total nanocalorimetry signal and the contribution of different types of defects for a $3{\cdot}10^{14}$ cm^{-2} 10 keV Si implant at RT. The most of the signal corresponds bond defects and to a lesser extent to self-interstitial and vacancies and their cluster. Figure 3 shows the atomistic damage profile for the same implant, as implanted at 300 K and at 1020 K. At low temperatures, the heat is mostly released by clusters and small amorphous pockets that recombine in the tail of the damaged region. At higher temperatures the peak is associated to the regrowth of the continuous amorphous layer.

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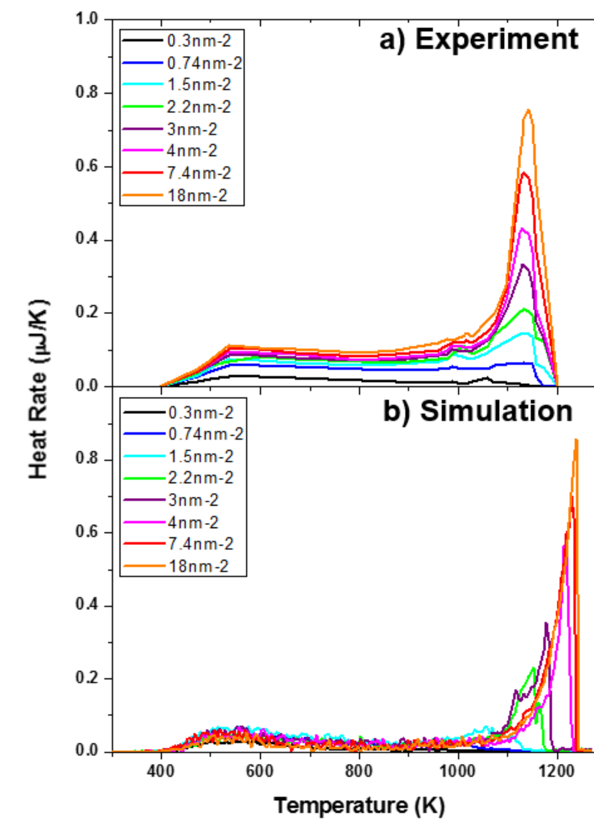

Fig.1. Heat release during damage annealing after implantation at 10 keV as a function of temperature for different doses.

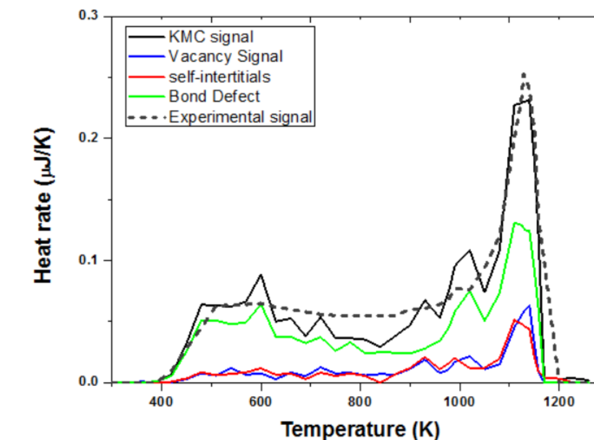

Fig.2. Heat release during damage annealing after implantation at 10 keV as a function of temperature for $3{\cdot}10^{14}$ cm^{-2}. Solid black lines: KMC model results. Dashed black lines: experimental results. The signal can the signal can be decomposed into contribution of different types of defect: red lines are self-interstitials and their clusters, blue lines are vacancies and their cluster; and green lines are bond defects.

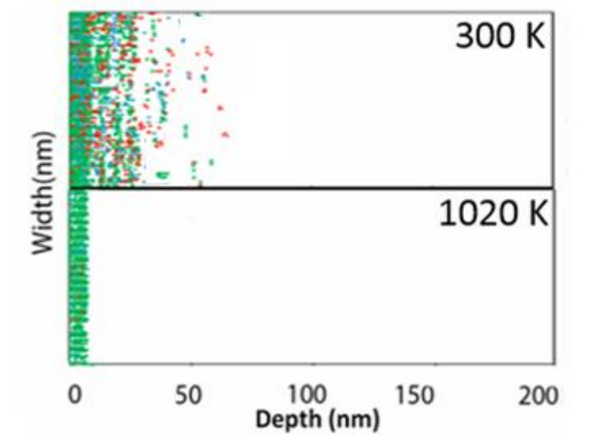

Fig.3. Atomistic damage profile for a $3{\cdot}10^{14}$ cm^{-2} 10 keV Si implant at RT and after annealing at 1020 K. Green dots are bond defects, Red dots are interstitials and blue dots are vacancies.

MD simulations of vacancy-like defects in amorphous Ge

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1. Introduction

The formation of nanostructures or porosity in semiconductor materials has potential applications for energy storage, photovoltaics, chemical sensors or drug delivery [1]. Nanoporous Ge, consisting of big cavities of nanometer sizes surrounded by thin walls, usually referred as *honeycombs* voids [1], is formed when an amorphous Ge (aGe) layer is implanted with large doses of heavy ions in a temperature window (-80 - 200 ºC) [2]. Two theories have been proposed for the formation of *honeycombs*. One of them assumes that Ge interstitials (Is) would migrate to the surface resulting in swelling, without interacting with vacancies (Vs) which accumulate in voids [3, 4]. The other one argues that the microexplosions and the thermal spike process within implant cascades generate the seeds for big voids [5]. Some reports point out that local pressure may also play an important role [5].

In this work, we use molecular dynamics (MD) simulations to analyze the generation and diffusion of Vs in aGe, and the role of local pressure, as these mechanisms are key to understand the formation of *honeycombs*.

2. Simulation scheme

MD simulations were done with LAMMPS [6], using multi-component Tersoff [7] to describe the atomic interactions. Amorphous Ge was created by the melting and quenching of a cubic simulation cell of 10 nm side, under periodic boundary conditions in all directions and zero pressure. Melting was achieved by keeping the lattice at 5000 K for 100 ps. Liquid Ge was then slowly cooled down at a rate of 10^{11} K/s. Liquid and amorphous Ge were characterized by the radial distribution function and the comparison with experimental data. Local pressure was determined from the atomic hydrostatic pressure and the von Mises stress. The cell was heated at 1500 K under different external hydrostatic pressures to study defect diffusion.

3. Results

Defect identification inside amorphous layers is complicated since there is no crystalline template to compare with. We propose a method to identify Is and Vs in aGe based on the local distortions they induce (coordination defects, bond distances, etc.). Our simulations indicate that many Vs are quickly absorbed in the amorphous lattice, since some of their under-coordinated neighboring atoms move to restore full coordination. However, vacancy diffusion up to second neighbor distances is also observed (Fig. 1), especially under positive (compressive) pressure conditions. This result is supported by the data of Fig. 2, which shows the mean-squared displacement at 1500K in aGe with 1% of randomly distributed Vs. The presence of Vs increases diffusion, which is particularly enhanced under compressive external pressure. To analyze the formation of small voids, the aGe cell enriched with 1% of randomly distributed Vs was annealed at 1500 K for 1 ns. The snapshots reported in Fig. 3 show that negative (tensile) pressure may increase vacancy volume and favor the growth of voids.

To summarize, our MD simulations indicate that vacancy diffusion in aGe is limited, and underline the role of local pressure on the diffusion and accumulation of Vs.

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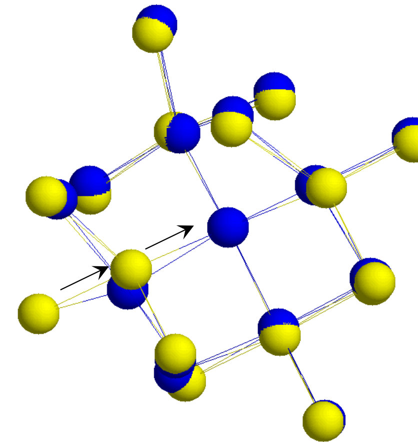

Fig.1. Vacancy diffusion to a second neighbor position. Initial and final atom positions are indicated by yellow and blue spheres, respectively. The arrows show the main atom displacements.

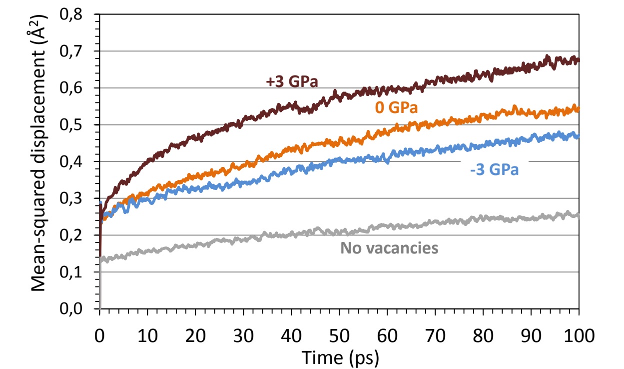

Fig.2. Mean-squared displacement at 1500K in an amorphous Ge cell with 1% vacancies under -3, 0 and 3 GPa of external hydrostatic pressure. Results for a reference sample with no vacancies and zero pressure are also included.

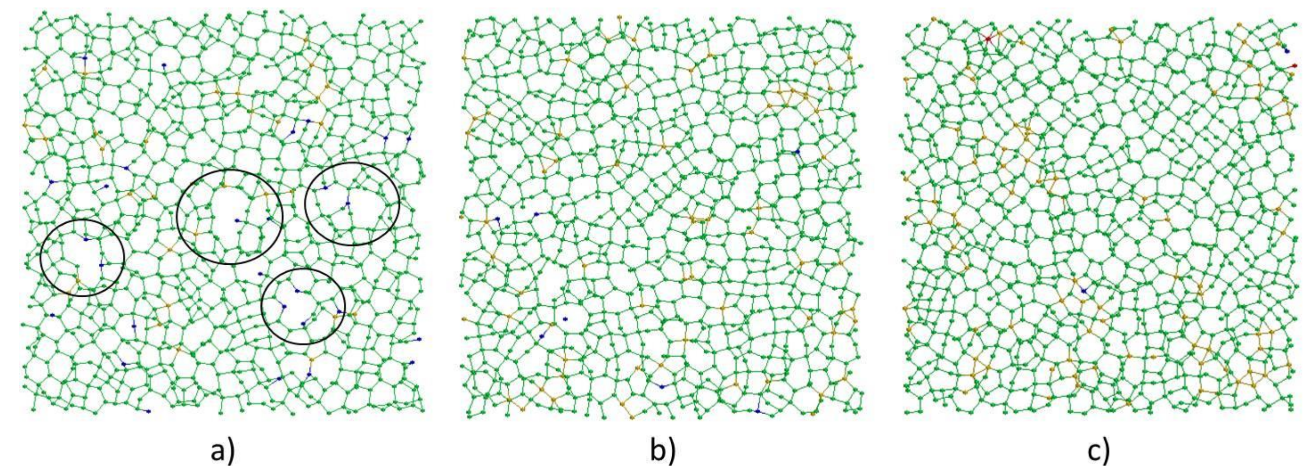

Fig.3. Slices with a thickness of one lattice distance of amorphous Ge with 1% of randomly distributed vacancies annealed at 1500 K for 1ns, under -3 GPa (a), 0 GPa (b) and +3GPa (c) of external hydrostatic pressure. Atoms are colored according to their coordination number: blue (3), green (4), yellow (5), and red (>5). Black circles indicate the presence of vacancy clusters at -3GPa.

Optoelectronic properties of embedded silicon nanocrystals by hyperspectral low-loss EELS

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1. Abstract

We will present an advanced data analysis method for the characterization of silicon nanocrystals (Si-NCs) embedded in dielectric matrices by high angle annular dark field (HAADF) and electron energy loss spectroscopy (EELS). The growth mechanism for these particles starts with a multilayer stack of alternated stoichiometric and Si-rich silicon-based dielectric material layers. The following dielectric materials and their silicon-rich counterparts were used; SiO2, SiC and Si3N4. Upon annealing, the Si-NCs crystallization is achieved, confined to this dielectric media. Because of this mechanism, these particles are always embedded in dielectric material. The experimental part of this work has been performed in an aberration corrected scanning transmission electron microscope (STEM), equipped with a monochromator. This set-up ensures the necessary high spatial and energy resolution for the characterization of particles whose size is below 5 nm.

Hyperspectral analysis techniques have been employed, based on the HAADF-EELS spectrum image (SI) acquisition. Plasmon energies determined at EELS-SI reveal the approximate spatial distribution of the Si-NCs and barrier dielectric materials. Three different samples were tested, depending on the case. SiO_2, SiC and Si_3N_4 all showed a higher plasmon energy and broader peak than crystalline Si. This method is better suited than the examination of the HAADF images, because of the closeness of the effective atomic number (Z) for all these species. Also, the appearance of spurious features from the inhomogeneity of the sample will mask the Si-NC positions (see Figs. 1 and 2). It is never possible in these cases to get a direct measurement of the contribution of the Si-NC to the spectra: all measured data present at least a mixture of nanoparticle and substrate plasmons. Fitting of these two peaks using a double plasmon model (DPM) is reliable only when they are well separated in energy and exhibit significant differences in FWHM, i.e. low energy narrow peak vs high energy wide peak. We have previously showed that this is possible in some cases [1], like for Si-NCs in a SiO_2 substrate. However, for other non-favorable situations, this approach does not ensure a good result while requiring a great effort. In these situations, segmentation of the EELS-SI by mathematical morphology (MM) can be of great help [2]. Following this scheme, averages of the spectra in the particle and dielectric areas can be generated, along with slices of the EELS-SI. These slices are then analyzed using multivariate analysis (MVA) algorithms (NMF and BLU) for a factorization of the EELS data (see Fig. 3).

In this sense, the generation of maps from measured properties on the spectrum, such as characterization of the plasmon peak and relative thickness from the measured spectra was complemented with segmentation of the EELS-SI using MM and a detailed exploration of spectral factorization using MVA. The collection of computational tools enabling nanometric spatial resolution imaging of the Si-NCs using sub-eV energy resolution EELS will be presented. Maps of measured properties, such as mean free path to sample thickness ratio, will be plotted for the three studied systems with different dielectric barriers. Moreover, the extraction of particular features by segmentation and factorization of the EELS data will allow recovering the pure Si-NC plasmon in each sample. Finally, the possibility of extracting electro-optical properties by thickness-normalized Kramers-Kronig analysis of the spectra will be explored.

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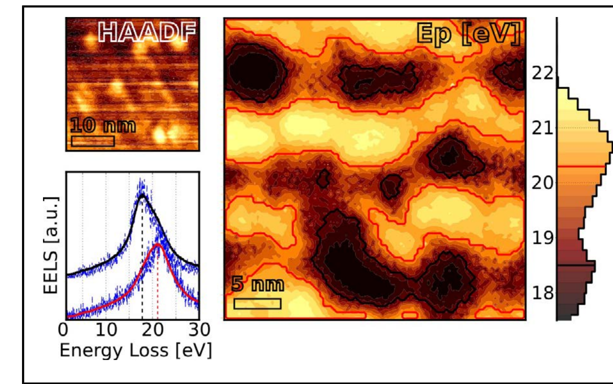

Fig.1. HAADF (upper left panel) and EELS (blue dashed lines, lower left panel) simultaneously acquired of a SiC sample. The EELS is analyzed to form the plasmon energy map (central panel, with thresholded histogram at left). Si-NC and SiC regions are marked off in this map and the average EELS are overlayed to the raw EELS (black=Si-NC, red=SiC).

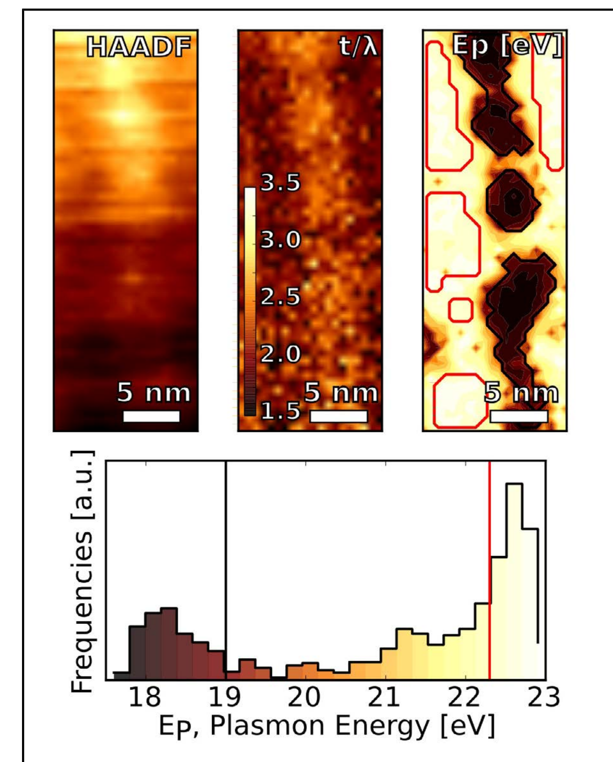

Fig.2. Results from the SiO_2 sample, showing the superior sensitivity of the plasmon energy map above the HAADF and relative thickness map. Si-NC and SiO_2 positions are marked off in the map and in the histogram (lower panel) as thresholds, using the same color code as Fig. 1.

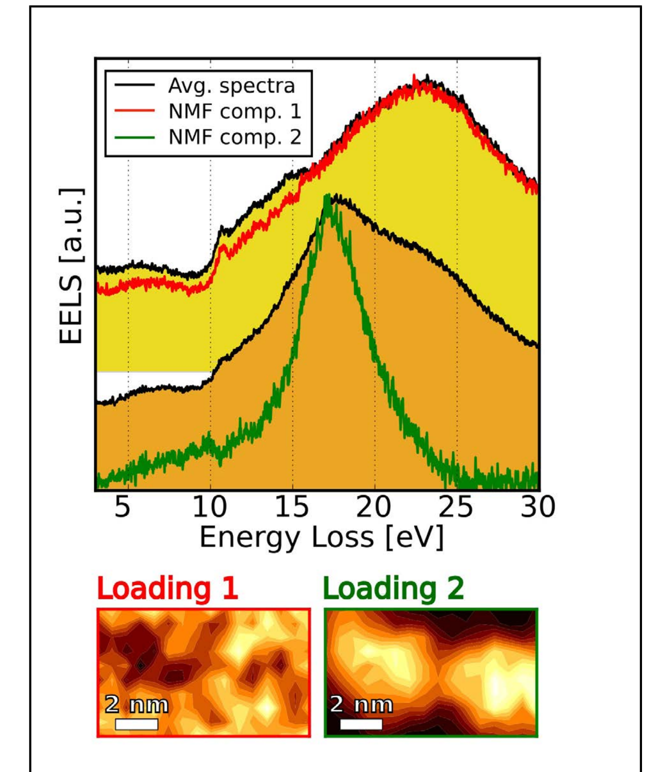

Fig.3. MVA factorization results vs. average EELS from the same EELS-SI shown in Fig. 2. After segmentation of the upper Si-NCs region, factorization reveals two different nanoparticles, and their contribution to EELS (comp. 2) is separated from the background SiO_2 spectra (comp. 1).

Valence EELS analysis of multiple InGaN-QW structure for electronic properties

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1. Abstract

We present a thorough study of InGaN quantum well (QW) structures at the nanoscale. These structures nominally consist of ~1.25 nm QWs layers with 20% indium content, periodically distributed along ~6 nm InGaN barriers, with 5 % indium content. Because of the structure reduced dimensions, the characterization required the best analytical scanning transmission electron microscopy (STEM) tools available. The ability of electron energy loss spectroscopy (EELS) to extract information about the electronic properties of the examined material is combined with structural characterization with high angle annular dark field (HAADF). Finally, the use of an aberration corrected STEM machine equipped with a monochromator ensures the optimum spatial and energy resolution of our maps and spectra.

When in STEM mode, HAADF and EELS can be performed simultaneously. High resolution HAADF images give structural information from the examined crystal lattice below the nanometer range. Z-contrast in these images reveals the position of the QWs, the occurrence of In diffusion or even the formation of In-rich islands. Moreover, this information can be exploited using geometric phase analysis (GPA) algorithms in order to obtain maps of the deformation along lattice directions. The resulting deformation maps reveal that the structure suffers a localized distortion along the growth axis related to the In-rich QW positions (see Fig. 1).

STEM-EELS spectrum images (SI) are used to gain insight into the material properties of the sample. For this purpose, maps of plasmon peak energy and width are obtained and compared with the HAADF images. Generally, for III-V materials, compositional information can be recovered from the analysis of the plasmon peak energy through Vegard law [1]. In the present case, the small size of the examined QW and plasmon delocalization make this approach difficult to apply. However, the analysis of the plasmon witdth reveals a consistent swelling of the peak related with the position of In-rich regions, along with some expected shift to higher energy (see Fig. 2).

Furthermore, Kramers-Kronig analysis (KKA) of the EELS allows recovering the complex dielectric function (CDF) which contains electro-optical information from the material. For instance, it is possible to calculate the electron effective mass (m*) from the recovered CDFs at each pixel of the EELS-SI [2]. The obtained values of m*, ranging from 0.14·m0 to 0.18·m0 are among the expected for InGaN (m*GaN = 0.2·m0 m*InGaN=0.11·m0). Moreover, depression regions in which the m* values are consistenty lowered are found in regions related with the ones having wider plasmon peaks (see Fig. 3).

All the computational work has been performed using the Hyperspy [3] toolbox. The collection of techniques that have been developed in order to perform these analyses, will be presented along with the obtained results.

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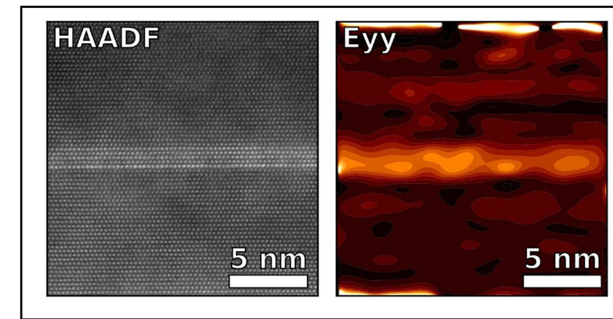

Fig.1. Left panel, HAADF-STEM image of the structure, revealing the position and width of an In-rich QW. Right panel, deformation in the growth direction calculated from the previous image by GPA.

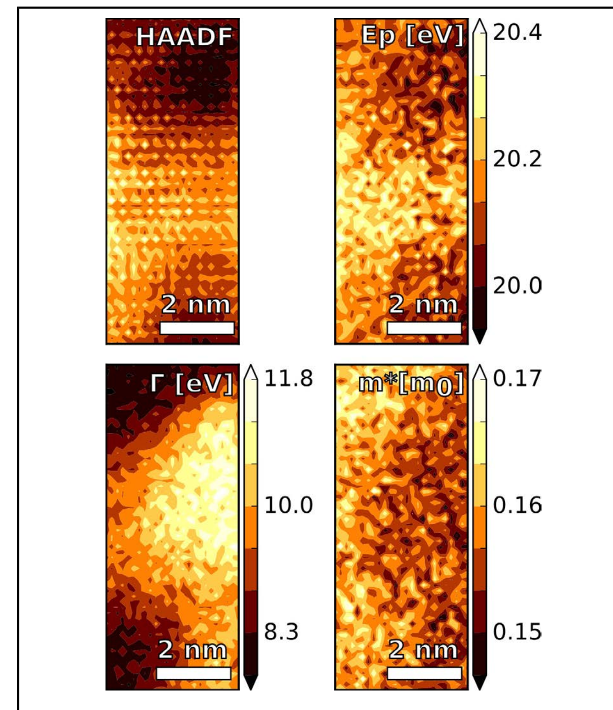

Fig.2. HAADF image and results from the analysis of the simultaneously acquired EELS-SI on an In-rich QW region. The plasmon analysis reveals a shift towards higher energies (Ep) and a swelling (Γ) of the plasmon peak around the QW. The effective mass (m*) shows a characteristic depression around the same region as the swelling in Γ.

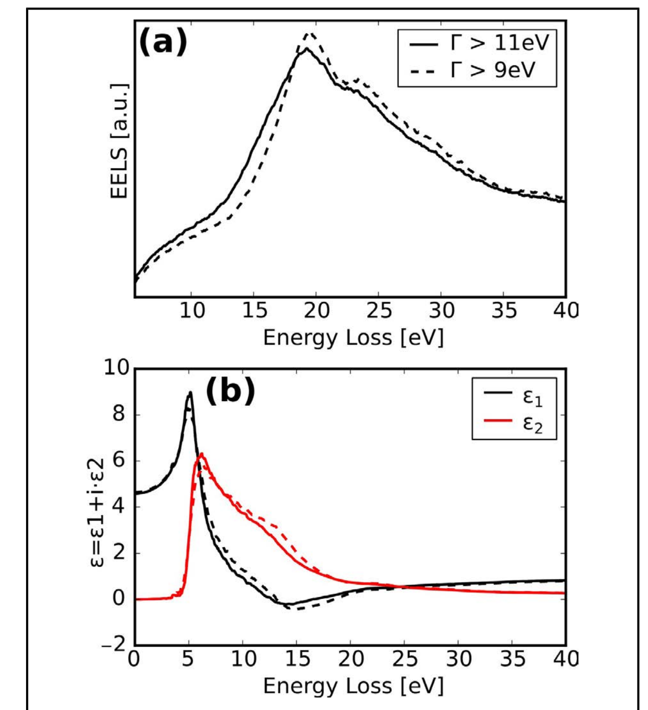

Fig.3. The upper panel shows two average EELS in the narrow Γ (dashed line) and wide Γ (solid line) regimes. Also following this line code, the lower panel shows the real (red) and imaginary (black) parts of the average CDF from these same regions.

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Straightforward Determination of the Effective Mobility-Lifetime Product of Small Molecule Organic Solar Cells

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1. Abstract

The effective mobility-lifetime product ($\mu\tau_{eff}$), a figure of merit for charge carrier transport in a photovoltaic device, was determined for small-molecule organic solar cells by a simplified methodology involving variable light intensity measurements. By use of a model that relates the recombination current density (J_{rec}) with the cell resistance at short-circuit (R_{SC}), the loss of performance in the intrinsic bulk heterojunction was correlated to lower $\mu\tau_{eff}$ values.

2. Introduction

Organic photovoltaics (OPV) have been the subject of intensive research during the last decade due to their low cost potential. Current challenges needed for their commercial success are 1) higher efficiencies and 2) longer operational lifetimes. To improve the efficiency is important to reduce the recombination losses, which are usually high in OPV. The mobility-lifetime product ($\mu\tau$) of charge carriers provides information about these recombination losses and is more suitable than other generic parameters (such as Fill Factor) as it relates to the active layer of the organic cell. Even though μ and τ can be measured or simulated by different experimental setups, they usually ignore recombination and the influence of other layers in the device (interfaces and electrodes). Consequently, this work describes a simple methodology for obtaining the effective $\mu\tau$ of a bulk heterojunction organic solar cell by measuring its response at different light intensities.

3. Experimental

Small molecule solar cells with the structure glass/ITO/MoO_3 (3 nm)/DBP:C_{70} 1:1 (x nm)/BCP (8 nm)/Al (150 nm) were fabricated by vacuum thermal evaporation at 10^{-6} mbar with an intrinsic (1:1 donor:acceptor ratio) active layer thickness x of 30 and 40 nm (Fig. 1). Electron donor material DBP was selected for its high absorbance and deep HOMO level of 5.5 eV (potential open circuit voltage $V_{OCmax} \approx HOMO_{DBP} - LUMO_{C70} \approx 0.9$ V) [1]. Active cell area was defined by mask at 0.075 cm^2 and characterization was carried under N_2-atmosphere. Variable light Intensity Measurements (VIM) were performed with an in-house experimental setup which measures the current density-voltage $J(V)$ response under different illumination intensities varied by neutral grey filters [2] (Fig. 2).

4. Results and Discussion

Fig. 3 depicts the standard 1.5AM (100 mW/cm^2) $J(V)$ response of the fabricated cells. As shown in Table 1, the device with 30 nm intrinsic (i) layer has a lower performance that could be attributed to a higher J_{rec}. To verify this, the resistance at short-circuit R_{SC} is extracted from the different VIM measurements (Fig. 4). It is observed that, over a wide range of light intensities, the $1/R_{SC}$ slopes meet at a single point referred as the collection voltage V_C. By differentiating the standard solar cell model (Fig. 5) and evaluating it at short circuit conditions, a $R_{SC}(J_{rec})$ relationship is obtained:

A charge-dependent mobility memristor model

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1. Abstract

In this paper we propose a new approach to the modeling of memristors, based on a non-constant mobility. This mobility, dependent on the trapped charge inside the memristor, enables modeling the memristor from physical principles, with no need of additional window functions. Simulations show that the model reproduces fairly well the expected behavior of a memristor, from physical principles.

2. Introduction

Leon Chua stated in [1] the existence of the passive element called Memristor in 1971, mainly based on theoretical arguments. The original reasoning was based on a missing element relating the electric charge and the magnetic flux, that would complete the symmetry of passive electronic devices. This first definition was extended later to include other elements whose resistance depended on a state variable. The first actual implementation of memristors was in 2008 [2], and it started a new interest, given their wide range of applications in digital and analogue circuits.

There are a number of approaches that aim to model the memristor behavior attempting to characterize both current/voltage behavior and the device dynamics. The first model describing the behavior of an actual memristor was presented in [2], and the memristor is described as a device with two differently doped layers of variable size. This size changes with the charge passing through it, thus changing the characteristics of the device. This model has been followed by many other models, all of them using a similar approach [3-8]. All these models share a common weak treat, which is their dependence on how they deal with the change of the size of each region, using what are called window functions. In this work, we propose a new approach that does not need using these kind of functions and is still physically based.

3. Description of the model

It has been described in [9] that the mobility in certain materials is strongly dependent on the concentration of carriers. Specifically, one of those materials is TiO2. Thus, we wanted to check if memristors could also be modeled using this effect. To do so, we have modeled the mobility using a charge dependence:

$$\mu = \mu_0(1 + q_a Q)$$

Where qa is a fitting constant that takes into account the effective change in the mobility due to the trapped charges, and Q is the integral of the current that has gone through the device:

$$Q = \int i(t)dt$$

Then, the resistance R of the memristor is modelled as:

$$R = \frac{L}{A}\frac{1}{qN_D\mu} = \frac{L}{A}\frac{1}{qN_D\mu_0(1 + q_a \int i(t)dt)}$$

Where L and A are the length and the area of the effective conductance path, ND is the effective doping of the channel, and q is the electron's charge.

4. Simulations

The model has been implemented in Verilog-AMS, using the Cadence suite. In order to validate the model, we have first of all checked the presence of a hysteresis cycle. Fig. 1 shows that it is present, and the amplitude of the hysteresis changes with the frequency, as it must. Fig. 1 shows this behaviour for three different frequencies.

The actual resistance of the memristor is governed, like in a normal semiconductor, by the effective doping of the conductive path, and the mobility of the carriers. Fig. 2 shows the changes when these parameters are changed.

Finally, it has to be noted that this model can fit both P- and N- type memristors, by changing the sign of q_a. Fig 3 shows the temporal evolution of two different memristors with all their parameters identical, but the sign of q_a. It is clear that the evolution of the signals are temporally mirrored.

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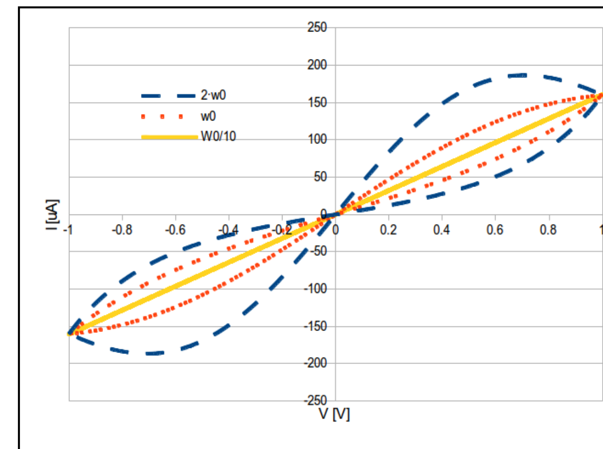

Fig.1. Behavior of the model for different input waveform frequencies, referred to a given frequency.

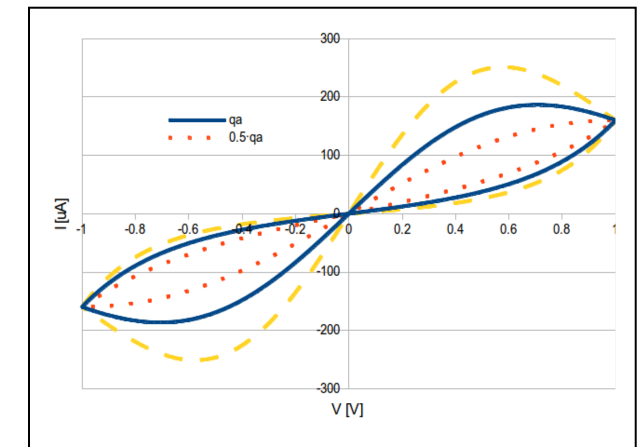

Fig.2. Dependence on the value of the parameter qa for different ratio values of 1.5, 1, and 0.5 of a given qa.

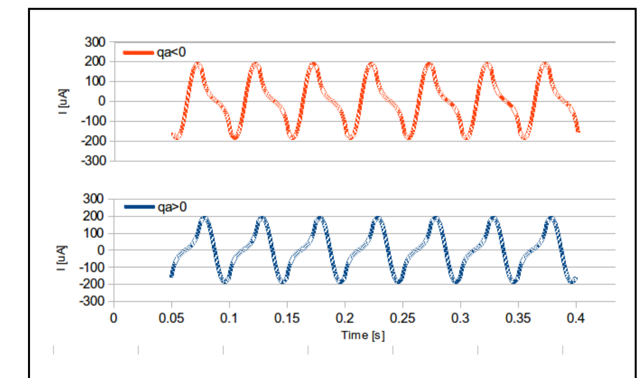

Fig.3. Change of behavior from P- to N- type by changing the sign of the qa parameter. The upmost signal has been generated by a memristor with positive qa, while the lower signal corresponds to a negative qa.

Piezoresistive cantilever force sensors based on polycrystalline silicon

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1. Abstract

We report the fabrication of polycrystalline silicon piezoresistive cantilevers with submicron width and thickness for static force measurements, using electron beam lithography (EBL) and silicon micromachining. For cantilevers with length of 150 µm, leg width of 500 nm and thickness of 320 nm, a force sensitivity of 97 µV/pN and a resolution of 30 pN have been obtained. Bigger cantilevers (leg width 6 µm, thickness 650 nm) fabricated with nominally identical processing conditions have shown a lower resistivity and a higher gauge factor. We show that the differences result from an increased effect of the grain boundaries for the smaller cantilevers. But these have a better force sensitivity and resolution due to their reduced lateral dimensions.

2. Introduction

Micromechanical cantilevers were originally developed as probes for atomic force microscopy but have been later used for (bio)chemical sensing [1]. Piezoresistive detection [2] of the deflection has some advantages over the standard optical method. We have been developing piezoresistive cantilevers in polycrystalline [3,4] or crystalline silicon [5] for force measurements of biomolecular recognition [6]. This requires a force resolution < 100 pN. We report some of our results for polysilicon cantilevers, which show that the material properties have a different effect on the electromechanical behavior of the devices depending on their size.

3. Cantilever fabrication

On a 400 nm-thick silicon dioxide on a silicon substrate, two polysilicon layers are deposited, separated by a thin SiO_2 (Fig. 1). Both layers are doped by phosphorus ion implantation, plus annealed in N_2 at 1000C, so that they have a similar grain structure and therefore a similar intrinsic (compressive) stress and stress profile. The upper polysilicon is used as a piezoresistor. Two types of devices have been fabricated (Table 1 and Fig. 2), with optical or EBL lithography, with minimum cantilever widths of 2 µm and 400 nm, respectively.

4. Force sensitivity and resolution

The electromechanical response of the cantilevers has been characterized by applying a bending force with the tip of an AFM (Fig. 3). The deflected cantilever has been connected in a voltage divider configuration with an identical on-chip reference cantilever. A 5 V bias has been applied to the half bridge and the output has been amplified with a gain of 640. The results are reported in table 2.

5. Resistivity and gauge factor of polycrystalline silicon

Polycrystalline silicon is composed of small crystallites separated by non-crystalline grain boundaries. The gauge factor G of polysilicon was calculated by French and Evans [7]. The resistivity ρ and G result from the relative contributions of the grains and boundaries, e.g.

$$\rho = \frac{L - L_{gb}}{L}\rho_g + \frac{L_{gb}}{L}\rho_b$$

where L and ρ correspond to the grains and L_{gb} and ρ_b to the boundaries. We have calculated both ρ and G for our polysilicon (L=100 nm and a specific grain orientation texture), using known models for the various magnitudes. The result is shown in Fig. 4 together with the experimental results. We see that the effect of the grain boundaries is more important for the EBL cantilevers, which explains the changes in ρ and G.

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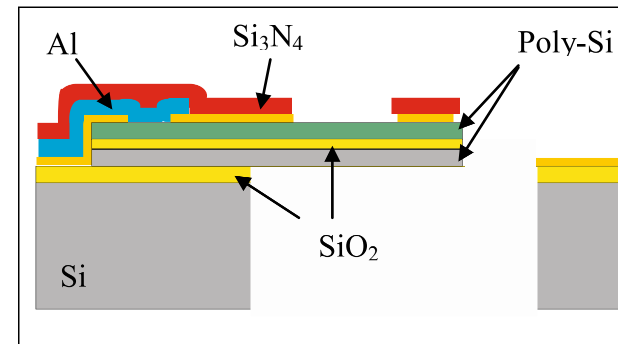

Fig.1. Schematic cross section of the fabrication process.

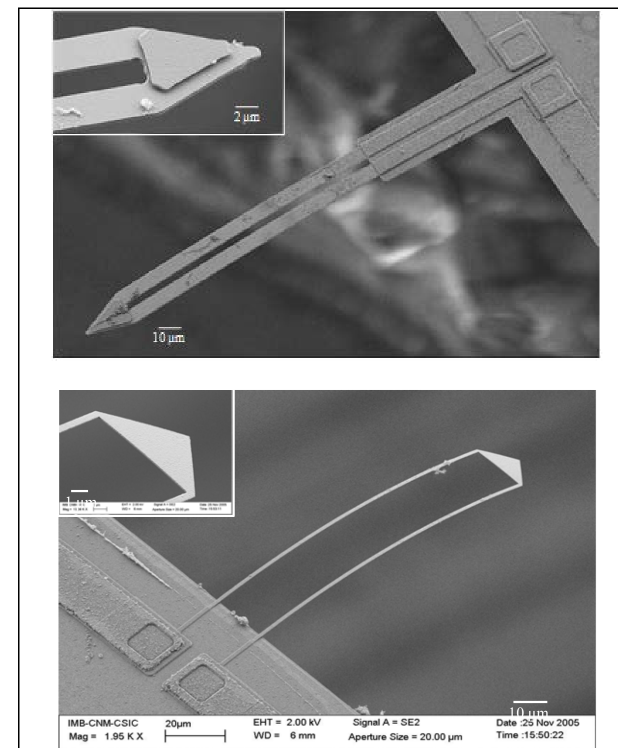

Fig.2. SEM micrographs. a) Polysilicon piezoresistive microcantilever (length 200 µm; leg width 8 µm; thickness 650 nm) and a cantilever tip (inset) with a silicon nitride platform. b) Submicron (600 nm) wide polysilicon piezoresistive cantilever defined by electron beam lithography, and a detail of the tip (inset).

Lithography	Optical	EBL
Poly 1 thickness	420 nm	220 nm
Inter-poly oxide	20 nm	7 nm
Poly 2 thickness	210 nm	110 nm
Poly Doping	$8\cdot10^{14}$ cm^{-2} / $4\cdot10^{14}$ cm^{-2}	$4\cdot10^{14}$ cm^{-2}/ $2\cdot10^{14}$ cm^{-2}
Length	150-300 µm	150-250 µm
Leg width	2-6 µm	0.4-1.0 µm

Table 1. Cantilever types, processes and dimensions

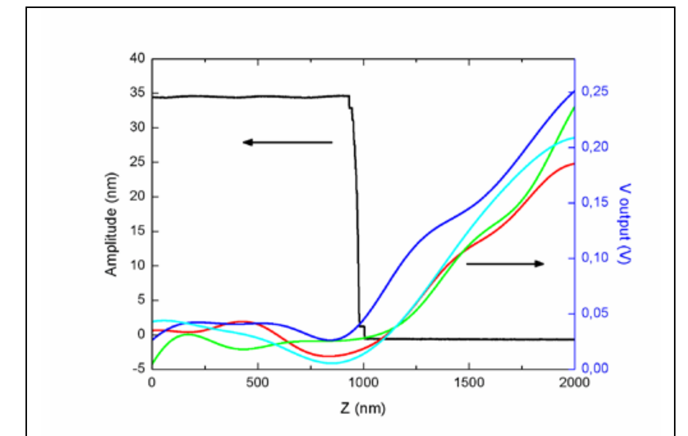

Fig.3. Output voltages of piezoresistive cantilevers, and amplitude of the oscillation of the AFM probe used to deflect them, for two sets of experiments (approaching and retracting the AFM probe), as a function of the vertical position. Each curve is an average of 20 actual measurements.

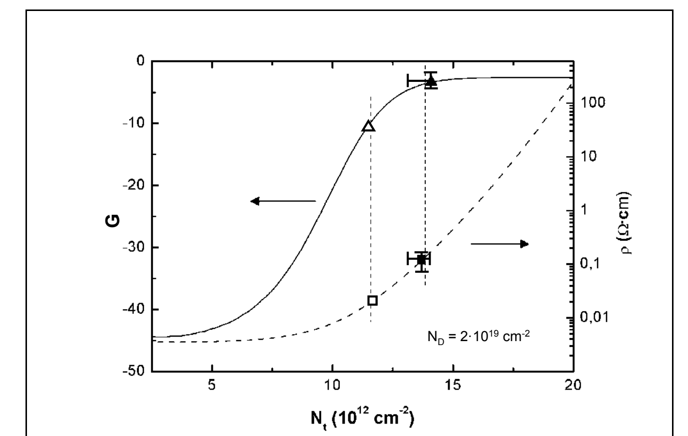

Fig.4. Calculated resistivity ρ (dashed line) and gauge factor G (continuous line) as a function of the trap density Nt in the grain boundaries, for a simple polycrystalline silicon model. A low Nt means that the material is dominated by crystalline grains, whereas for a high Nt the disordered grain boundaries dominate. The square and triangle points show the experimental ρ and G, respectively, for the wide (empty symbols) and narrow (solid symbols) cantilevers. There is only one adjustable parameter, a factor on the barrier piezoresistive coefficients, which moves up or down the high-Nt part of the G curve.

Cantilever type	Optical litho	EBL
Dimensions (Length x leg width)	220 µm x 6 µm	150 µm x 500 nm
Resistivity (Ω·cm)	0.021± 0.001	0.12 ± 0.05
Gauge factor G	-10.6 ± 0.7	-3.3 ± 1.3
F sensitivity	9.2 µV/pN	97 µV/pN
Output noise	750 µV	3.3 mV
F resolution	81 pN	30 pN

Table 2. Experimental results. The sensitivity includes an amplification gain of 640. The noise is calculated in the frequency range 50 Hz - 1 kHz.

Low Gain Avalanche Detectors for High Energy Physics Experiments

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1. Introduction

Low Gain Avalanche Detectors (LGAD) represent a remarkable advance in high energy particle detection, since they provide a moderate multiplication (gain ~20) on the collected charge, thus leading to a notable improvement of the signal to noise ratio, which largely extends the possibilities of application of silicon detectors beyond their present working field. This work summarizes the design and optimization aspects of the LGAD detectors fabricated at the IMB-CNM clean room, as well as the main results of the characterization tests performed in several laboratories and institutions assigned to the CERN RD50 collaboration [1].

2. Low Gain Avalanche Detectors

Based on the standard PiN diode design, the $P^+/\pi/P/N^+$ structure of the LGAD (Fig. 1) includes a moderately doped P-type diffusion beneath the N-type electrode, which allows the generated charges to undergo avalanche multiplication before being collected. In this sense, the LGAD perform is analogous to that of the Avalanche Photo-Diode (APD), normally used for optical and X-ray detection [2]. However they show a lower gain value on the output signal (~20, against 100-1000, or even higher, for APD), which makes LGAD more suitable for the detection of high energy charged particles. In contrast with the APDs, detected signals are moderately increased in LGADs, without significant increase of the noise levels, thus improving the signal-to-noise ratio of the detector. In addition, LGAD detectors offer the possibility to have fine segmentation pitches, thus allowing the fabrication of micro-strip and pixel devices, which do not suffer from cross-talk in their readouts.

The LGAD core region, as depicted in Fig. 1, is provided with a proper edge termination design, consisting of a deep N-type diffusion, which overlaps the lateral curvature of the multiplication junction, preventing a premature cylindrical breakdown, as well as ensuring the stability and uniformity of the electric field distribution across the whole junction area (Fig. 2). In addition, the peripheral region includes several elements to avoid the collection of the surface component of the current, which is normally considered a noise source, since it is not generated by the incident radiation. A collector biased ring (Fig. 3) confines the sensitive volume of the detector to the core region, since most of the charge carriers generated outside are extracted separately by the ring. Besides, P-stop and P-spray diffusions are placed within the peripheral region (Fig. 4) to avoid the undesirable effects derived from the surface inversion of the substrate, produced as a consequence of the accumulation of positive charges in the peripheral oxide.

3. Prototype Performance

First LGAD prototypes were fabricated at the IMB-CNM clean room on 300 µm-thick wafers [3], and subjected to various characterization tests in several laboratories of the CERN RD50 collaboration. The evaluation of the charge collection efficiency with a β-particle ^{90}Sr source (Fig. 5), have shown an excellent detection performance, with gain values in the range of 10-20, while the noise signal remained comparable to that of a commercial PiN diode. Transient Current Technique (TCT) analysis with laser and α-particle sources have revealed the collection dynamics and stressed the high uniformity of the multiplication process within the junction area (Fig. 6).

Finally, LGAD samples subjected to high fluence neutron (Fig. 7) and proton irradiations have shown a notable reduction in their collection efficiency, thus showing that the multiplication process is degraded when the detector is operating under harsh radiation conditions.

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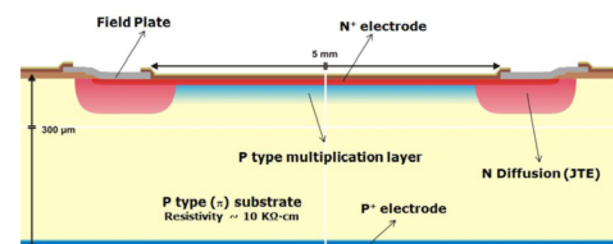

Fig.1. Schematic cross section of the LGAD core region, with the P/N^+ multiplication junction properly protected with a deep N-type diffusion, which overlaps the junction edges, preventing premature breakdown of the junction.

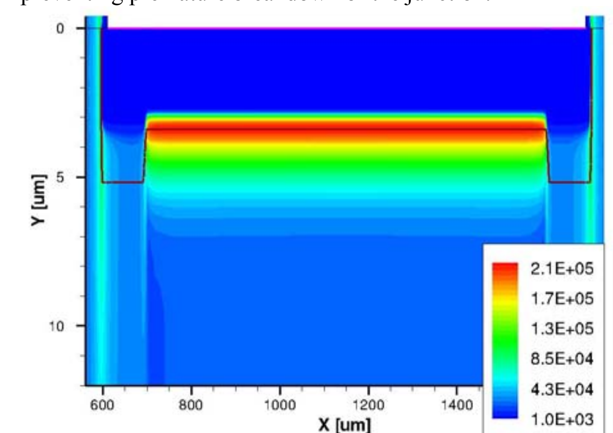

Fig.2. Simulated electric field distribution at a reverse bias of 400 V within the core region of a LGAD detector.

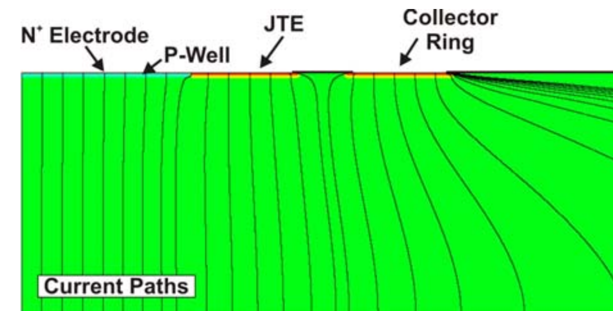

Fig. 3. Simulated current paths on a LGAD structure provided with a collector ring to individualize the bulk and surface current readout.

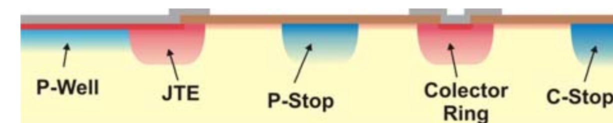

Fig. 4. Schematic design of the LGAD peripheral region, with P-Stop and C-Stop diffusions suitable placed to prevent the formation of a surface inversion channel, below the field oxide.

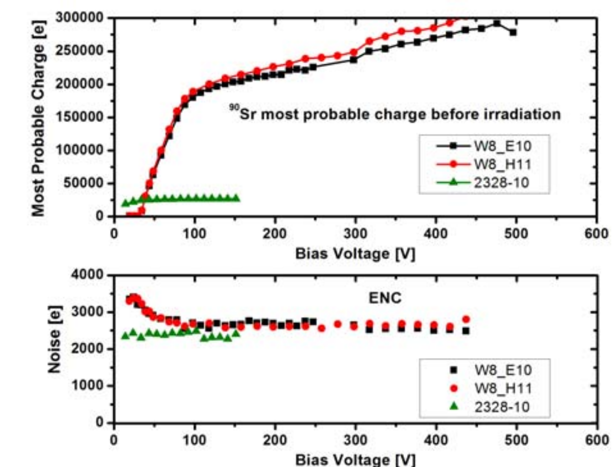

Fig. 5 Most probable value of the collected charge (up) and Equivalent Noise Charge (ENC) (down) measured in two LGAD samples exposed to a 90Sr electron source, compared with the outcoming signals of a commercial PiN diode.

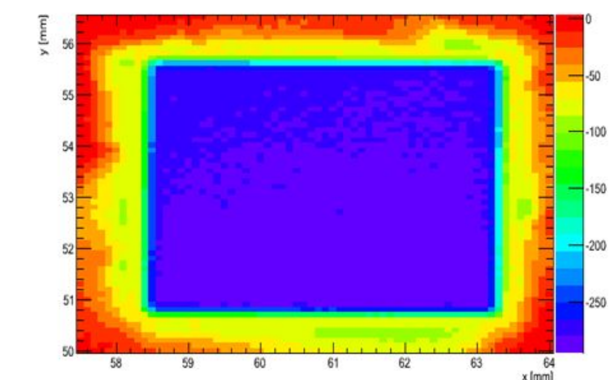

Fig. 6 Charge collection and multiplication uniformity evaluated on a LGAD sample with the TCT technique applied with a red laser in steps of 100 µm to cover the whole detection area.

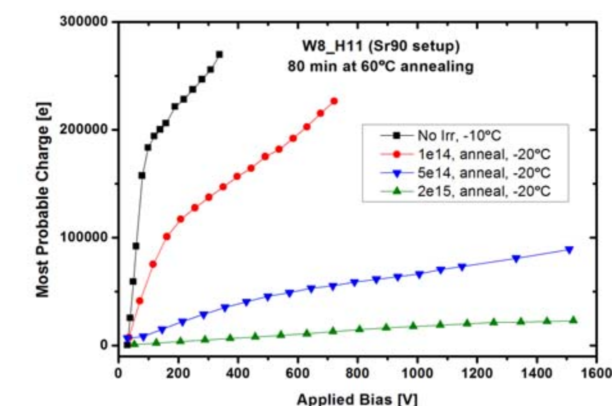

Fig. 7 Reduction of the collected charge in a LGAD prototype subjected to different fluences of neutron irradiation, as a consequence of the degradation of the multiplication process.

Anomalous Low-Frequency Noise Increase at the Onset of Oscillations in Gunn Diodes

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1. Abstract

In this work, the presence of anomalous low-frequency noise effects in Gunn diodes has been studied and evidenced. Near the onset of Gunn instability, there is a limited range of bias voltages for which the noise significantly increases at frequencies well below the frequency of oscillation. For higher bias voltages, the oscillation becomes purer and such low-frequency noise drastically vanishes.

2. Introduction

Gunn diodes have been commonly used in the implementation of microwave oscillators. Nowadays, Gunn devices working up to several hundreds of GHz can be found in the literature [1], and even some recent studies consider structures prospectively able to oscillate at THz frequencies [2].

A Gunn diode oscillates when a bias voltage above certain threshold is applied to the device. However, between the initial static state and the generation of a purely periodic signal there exists a voltage range for which incoherent fluctuations appear. In the last case, when uncorrelated instabilities are formed, one of the effects that can be observed is an anomalous increase of the noise at very low frequencies. This phenomenon has been reported in some experimental works based on GaAs devices [3]-[4], although restricted to a very limited frequency range. More recently, similar results were also reproduced for InN, InGaAs, InP and GaN diodes using Monte Carlo simulations [5]-[7].

The origin of such critical enhancement of the low-frequency noise is attributed to the existence of intermittent oscillations for a given range of voltages, preceding the formation of a coherent oscillation [4],[8]. The objective of this work is to analyze this effect in more detail by combining Monte Carlo simulations and experimental measurements performed in InGaAs diodes.

3. Results and comments

In a first approach, the noise characteristics of a Gunn diode have been studied by means of a home-made software tool based on the Monte Carlo particle method. The simulated device is a one-dimensional InGaAs diode, with an active region of 4 μm length and doped 2×10^{16} cm^{-3}. A notch has been introduced at 1 μm distance from the cathode to facilitate the formation of the oscillatory domains. The simulated current spectral densities for different DC voltages are shown in Fig. 1. The frequency of oscillation is around 50 GHz. As it can be observed from the graph, the low-frequency noise significantly increases at V=1.65 V, when the oscillation begins to appear. For increased bias voltages, the oscillation peak increases whereas the low-frequency noise drastically reduces. Such phenomenon can be clearly observed in Fig. 2, where the current noise density at 3 GHz (low-frequency) for different bias voltages has been plotted.

In order to experimentally validate the previous results, the power spectra of a set of Gunn diodes have been measured in a wide frequency range [8]. The devices are InGaAs planar diodes, based on a structure similar to the one presented in [1]. For the measurement, a PNA-X N5244A with Option 029 from *Agilent Technologies* has been used, which allows acquiring the output power density from an electronic component with high levels of accuracy and sensitivity [9]. The measured power spectra of a diode with 3.1 μm channel length are shown in Fig. 3. The frequency of oscillation in this case corresponds to 30 GHz. Close to V=8.0 V, when the oscillation peak begins to be formed, a noticeable noise hump appears in the low part of the spectrum at around 400 MHz. The noise power density at 400 MHz as a function of the voltage is represented in Fig. 4. Again, when the bias voltage is increased, and the oscillation is well established, such low-frequency noise decreases.

Both simulated and experimental results exhibit a similar behavior and have been useful to further understand the low-frequency noise mechanisms that are present in Gunn diodes at the onset of oscillations. In practice, this knowledge can be used as an indirect method to predict higher-frequency oscillations in setups where a direct detection is a complicated challenge, as in the case of (sub-)THz Gunn oscillators.

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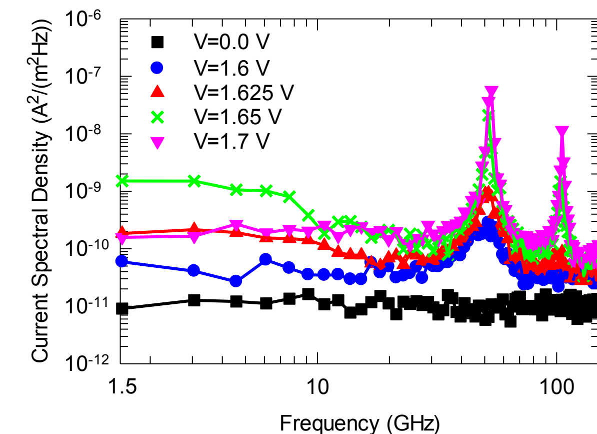

Fig. 1. Simulated current spectral density of a 1D InGaAs Gunn device for different DC voltages.

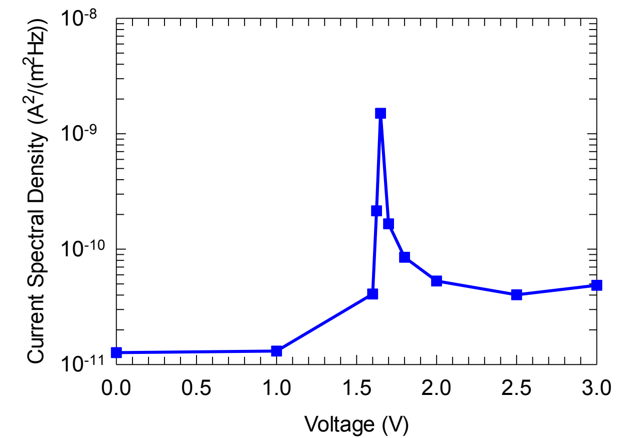

Fig. 2. Simulated noise current spectral density of the 1D InGaAs Gunn device at 3 GHz.

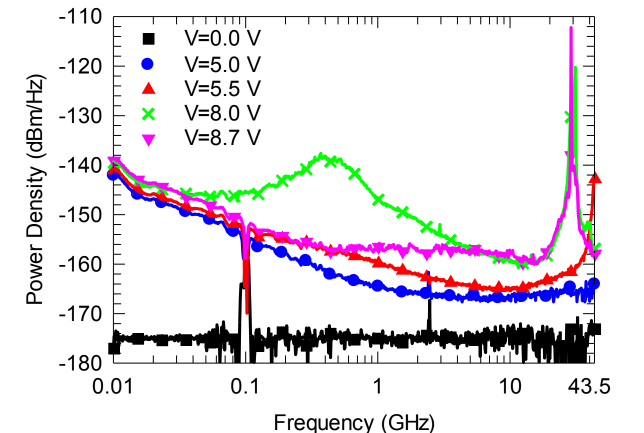

Fig. 3. Measured power spectral density of a 3.1 μm length planar Gunn diode for different DC voltages.

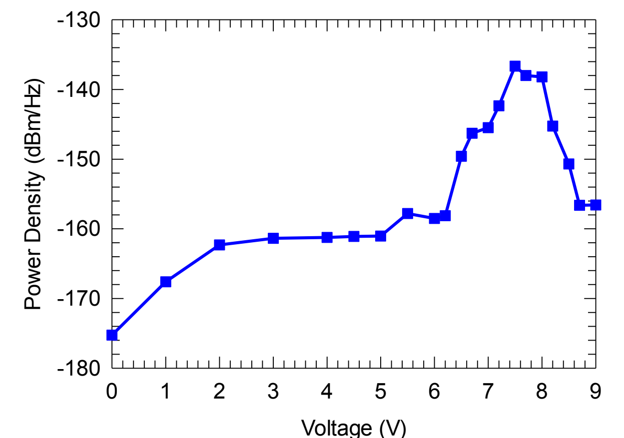

Fig. 4. Measured noise power spectral density of the 3.1 μm length planar Gunn diode at 400 MHz.

Real time detection of beer defects with a hand held electronic nose

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1. Abstract

A hand held wireless portable electronic nose (e-nose) has been developed for general purpose applications. It is based on non-specific micromechanized semiconductor sensors. It has been applied to the real time detection of two common aromatic defects in beer: acetaldehyde and ethyl acetate.

2. Experimental

The aroma of beer is important as a characteristic feature and for the quality of the product as well. The development of artificial sensors, such as electronic noses is a promising direction to evaluate the aroma of beers [1]. In this work, attempts were made in order to detect the change of aroma of beers adulterated with some common defects by using a metal oxide semiconductor based electronic nose.

A schematic of the e-nose and measurement setup is shown in figure 1a. It consists of two gas inlets that are switched through a three way electrovalve whose output is connected to the pump and the sensors cell. One of the gas inlets has a carbon filter for air as reference baseline. The whole system is controlled by a digital signal controller. Main measurement parameters are shown in a touchscreen LCD. Several rechargeable batteries give about 8 hours of autonomy to the e-nose.

The sensors cell and board are designed for microsensors in a TO-5 12 leads package but it is easily adaptable to other packages. A photograph of the e-nose is shown in figure 1b. Details can be found elsewhere [2].

The e-nose is controlled by a Labview program. It displays and controls the measurement parameters (temperature, sensor resistance, temperature, valve status, battery status, pump power). It automatically generates the response database. Principal component analysis (PCA) and probabilistic neural networks (PNN) have been implemented in Matlab for data analysis.

Two aromatic defects in beer have been measured acetaldehyde and ethyl acetate at level between the organoleptic threshold and five times this quantity. For acetaldehyde the threshold is 25 ppm and for ethyl acetate is 21 ppm [3, 4].

3. Results and discussion

Ten mL of each compound was placed in a 22 mL vial and kept at 18 ± 1 ºC by a Peltier system. A minimum of 10 replicates for each compound were measured. The response was calculated as the ratio between the sensor resistance in filtered air to the sensor resistance at the end of the sampling time. PCA were applied to these responses to see the data distribution among classes. Figure 2 shows the PCA score plots for ethyl acetate samples. Although there is confusion between classes it can be seen that the non-defect beer samples (blank) are separated from the ethyl acetate samples.

PNN and back propagation networks have been applied to the data in order to classify the samples. We have obtained classification rates over 80 % for both defects.

4. Conclusion

A hand held electronic nose has been applied successfully to the real time detection of beer aromatic defects such as acetaldehyde and ethyl acetate. Although it cannot quantify the defect content it can correctly classify the defective from the non-defective samples. Success classification rates of more than 80 % have been obtained.

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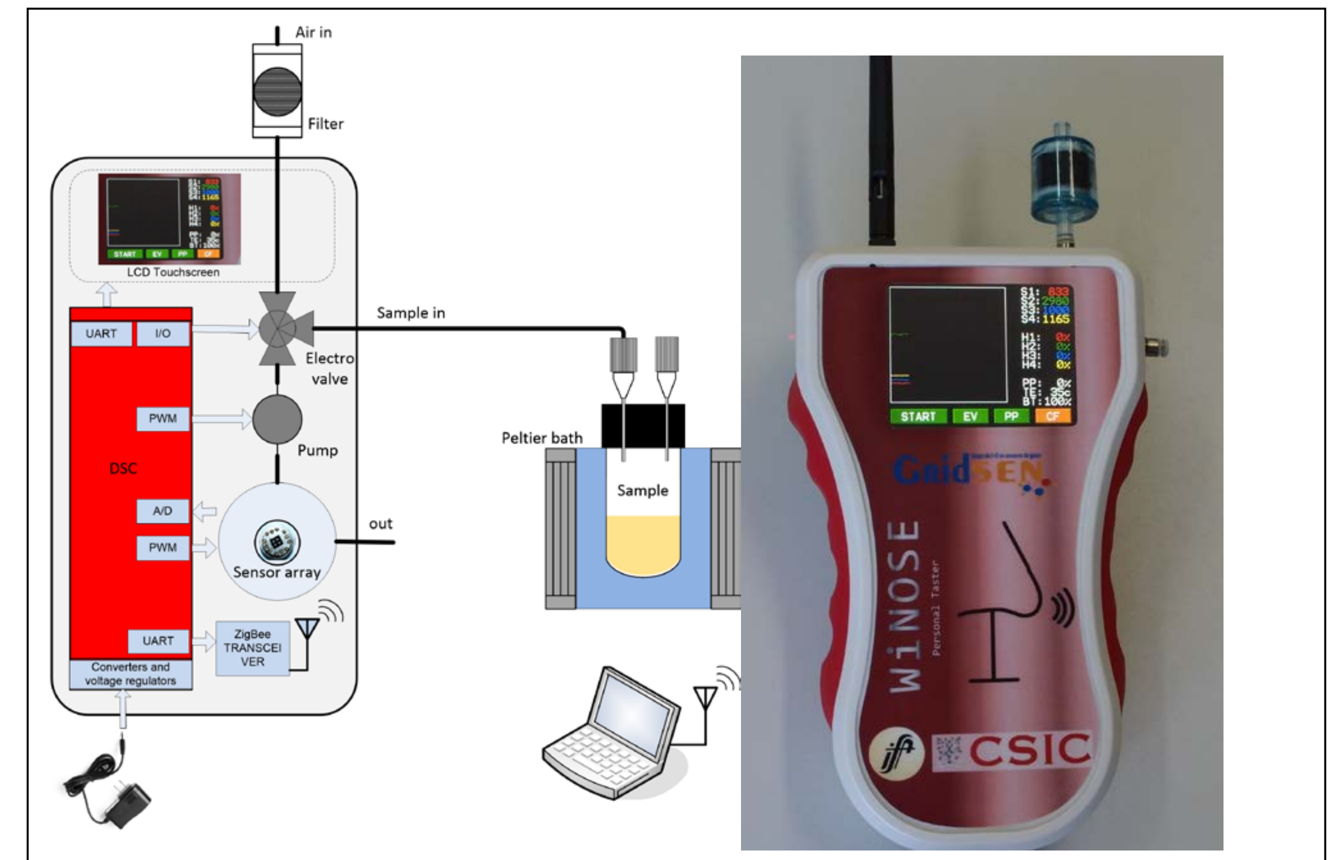

Fig.1. a) Electronic nose: a) Schematics with the measurement system b) Photograph

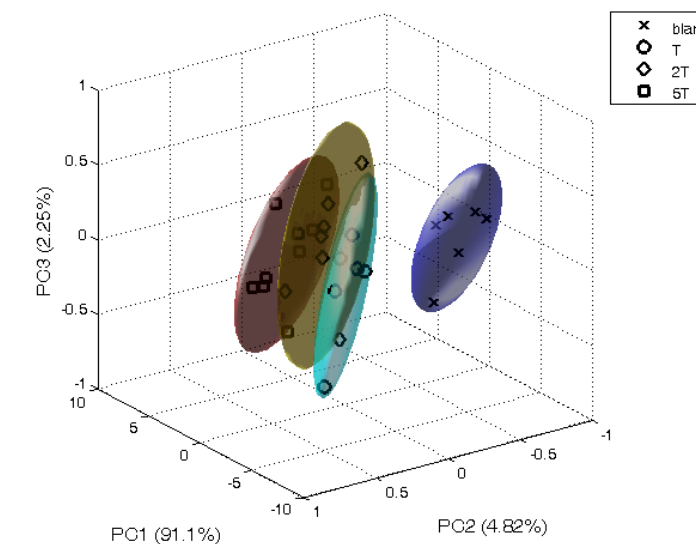

Fig 2. PCA plot for the ethyl acetate measurements in beer

Impact of NBTI and CHC stress on the nanoscale electrical properties of strained and non-strained MOSFETs

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1. Abstract

This work addresses the impact of BTI (Bias Temperature Instability) and CHC (Channel Hot Carrier) stresses on the different regions along the channel of the MOSFET gate dielectric. In particular, it is demonstrated that, while the BTI degradation is homogeneous, the CHC stress degradation is higher close to the source (S) and the drain (D). When comparing strained and non-strained channel devices, the results show that strained devices are more sensitive to CHC stress than non-strained ones.

2. Experimental

p-MOSFETs (W=0.5µm, L=0.13, 0.5, 1 and 3µm) with a 1.4nm thick SiON layer as gate dielectric have been analyzed. In strained devices, SiGe at the S/D regions was deposited with a 15% Ge content. Some samples were subjected to CHC stress by applying -2.6V at drain and gate, and some other were subjected to Negative BTI stress (NBTI) by applying -2.6V at the gate, while the other terminals were grounded. After 200s electrical stresses, the top electrode of the MOSFETs were removed for the nanoscale electrical measurements.

3. Discussion

First, the nanoscale effect of NBTI and CHC stress on the gate oxide electrical properties of non-strained MOSFETs has been compared. Fig. 1a-1c show, respectively, examples of typical current maps obtained at 3.6V on (a) non-stressed, (b) NBTI and (c) CHC stressed MOSFETs (L= 1µm). The measurable gate area has been delimited by a dotted line. Fig. 1d shows the averaged current profiles obtained along the channel for the three devices. After the electrical stress, brighter areas, corresponding to larger currents, were observed (which were related to NBTI and CHC degradation) while mainly noise level was measured in the non-stressed MOSFET. Moreover, the distribution of the leaky sites over the gate region is different for the different stresses. In the NBTI stressed MOSFET, the current shows a homogenous distribution along the channel. In the CHC stressed device, however, gate current is especially larger in the regions close to the source and drain, indicating a higher degradation (i.e, a larger defect generation) at these regions. The generated defects close to S and D can be attributed to NBTI and CHC degradation, respectively [4]. A quantitative analysis of Fig. 1 (see Table 1a) further supports these observations. Therefore, these results show that a CHC stress induces non-uniform degradation along the channel, being larger close to S/D.

The impact of a CHC stress on strained devices was also studied and compared to that on non-strained ones. Fig. 2 shows the current maps obtained at 4V on non-strained (a and c) and strained (b and d) CHC stressed MOSFETs, with L=3µm (a and b) and L=0.13µm (c and d). Larger currents can be observed in the gate area after the CHC stress compared to fresh devices (not shown), which is indicative of the induced degradation. In the 0.13µm MOSFET, currents can reach the maximum measurable value, indicating that BD was triggered during the CAFM scan. In the 3µm MOSFETs, however, the observed leaky sites are not BD spots and can be used to analyze the impact of the stress at the different channel regions. Table 1b shows the average gate current $\langle I_G \rangle$ measured on different devices (L=1µm) in regions close to the S, D and in the center of the channel, from images as those in Fig. 2. Close to S and D, currents are larger, demonstrating again the non-uniform degradation of the CHC stress. Moreover, currents are larger in strained devices, and especially, close to S/D. To quantitatively compare the impact of the CHC stress at the different regions of the channel on strained and non-strained devices, the β_G parameter was calculated (Table 1b), defined as $\beta_G=(I_{G,increase,\ strain} - I_{G,increase,\ non\text{-}strain})/\ I_{G,increase,\ non\text{-}strain} \times 100$. This parameter indicates the relative increment of the gate current in strained devices compared to non-strained ones. Note that β_G is larger close to S and D, showing that strained MOSFETs and, in particular, those regions subjected to strain (S and D), are more sensitive to CHC stress.

4. Conclusion

CAFM has been used to investigate the impact of CHC and NBTI stresses on non-strained and strained MOSFETs. After electrical stress, larger currents were observed at the gate area, which have been related to the induced degradation. In NBTI stressed devices the degradation is homogenously distributed along the channel, while in CHC stressed devices, degradation is higher close to S/D. These distributions were also observed in strained devices. Moreover, CAFM images have shown that stressed strained MOSFETs show larger currents, especially close to the junctions, demonstrating that they are more sensitive to an electrical stress.

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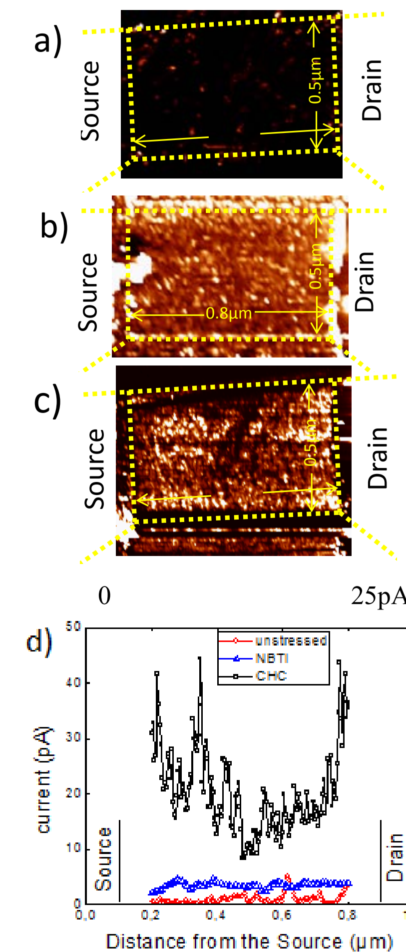

Fig.1. Typical current images obtained on a (reference) non-stressed (a), NBTI (b) and CHC (c) stressed MOSFETs (L=1 µm). (d) Average current measured along the channel for the non-stressed (circles), NBTI (triangles) and CHC (squares) stressed MOSFETs

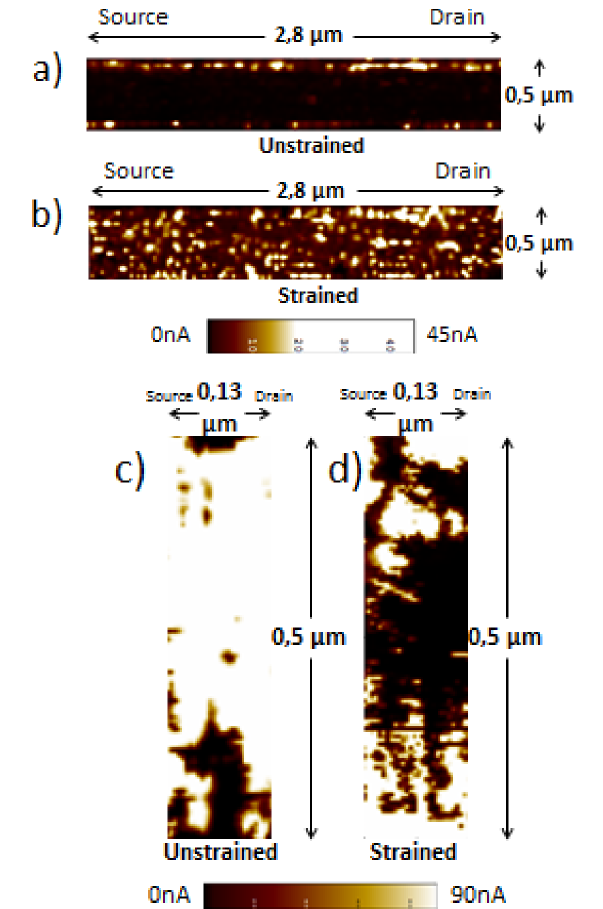

Fig.2. Current images obtained on a L= 3 µm (a, b) and 0.13 µm (c, d) MOSFETs with a non-strained (a, c) and strained (b, d) channel after CHC stress.

a)	Source		Center		Drain	
	<I> [pA]	σ_I [pA]	<I> [pA]	σ_I [pA]	<I> [pA]	σ_I [pA]
reference	0,4	0,1	1,1	0,2	1,1	0,9
NBTI	3,3	0,7	3,1	0,1	3,2	0,1
CHC	24,9	38,9	13,6	18,4	25,4	75,6

b)	$\langle I_G(nA) \rangle$		β_G
	Unstrained	Strained	
Source	2,67	10,54	294%
Channel	1,43	4,92	244%
Drain	2,01	9,51	373%

Table 1. (a) Average and dispersion of the current measured at a region close to S,D and in the center of the channel of Fig.1. (b) Average gate current $\langle I_G \rangle$ and β_G values obtained with CAFM close to S,D and in the center of the channel for strained and non-strained devices (L=1µm)

Microfluidic platform with absorbance sensor for glucose detection

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1. Abstract

In this paper, a microfluidic Lab on Chip (LOC) platform for clinical diagnosis of glucose is proposed. The method is based on measuring the amount of glucose in a blood sample using a colorimetric enzyme-kinetic method. The colorimetric changes are detecting using an absorbance system consisting of a light emitting diode and a phototransistor working in the wave length of 505 nm. The proposed platform is thought to be portable, it is designed over PCBMEMS and it is highly integrated with microfluidic platforms. The experiments have shown good stability of the measure due to the differential system.

2. Introduction

Glucose detection in human physiological fluids is an important issue in order to overcome the diabetes. In recent years, thanks to LOC devices, there have been several approaches [1-2]. However, due to his complexity these are not easily integrable in a multifunction microfluidic circuits, Fig.1. In this paper, a highly portable and integrable glucose detection platform is proposed.

3. Glucose detection

A working reagent is prepared dissolving the contest of enzymes, which will react with the glucose, with one Buffer (phenol). The reagent is mixed with the glucose in a DF=100. The intensity of the colour formed is proportional to the glucose concentration in the sample.

4. Optoelectronic system for detection

The optical detection setup consists of a green light emitting diode, a phototransistor and optional an instrumental amplifier. The system is measured in differential to avoid the ambient light noise. The setup is performed in a plane perpendicular to the microfluidic circuit. The voltage in the phototransistor is directly proportional to the light intensity incident and the light intensity is proportional to the absorbance.

5. Fabrication process and setup

The schematic of the platform can be seen in Fig.2. It consists on a PCB where the microfluidic circuit is found and a plastic structure, manufactured with 3D printing, where the diodes and phototransistors are integrated. The PCB with the microfluidic circuits contains two chambers of 5 mm where the different concentrations are located. This PCB is inserted in the plastic structure. Finally, this plastic structure is fixed to a PCB where the detection electronic is assembled.

6. Experimental results

In a first phase, the focus is on the optic circuit. A calibration with a cuvette of 1 cm light path is done to prove the validation and linearity of the system, as can be seen in Fig.3. In the second phase, experiments have been done with the complete setup. Three experiments were done with both chambers empty, both chambers full of reagent liquid and one chamber with reagent liquid and the other with Glucose of 100 mg/dl, Table.1. It was found that there is difference between liquid and glucose and can also be observed the stability of the system with a difference of only 11 mV from both chambers empty vs both chambers full of reagent liquid.

7. Conclusions

An integrable microfluidic platform for photometric glucose sensor has been reported. Due to the differential way of measurement and the plastic structure used to integrate the whole system, the reported device is greatly steady.

8. Acknowledgment

This work was supported by the Spanish Ministry of Science and Innovation under grants TEC2011-29045-C04-02, ISILAB.

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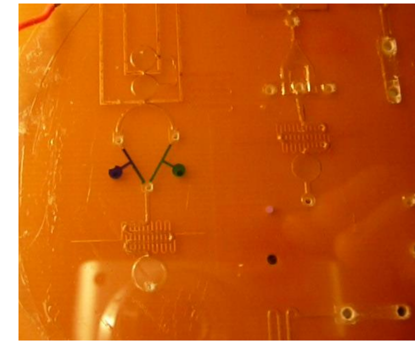

Fig.1. Multifunction microfluidic circuit

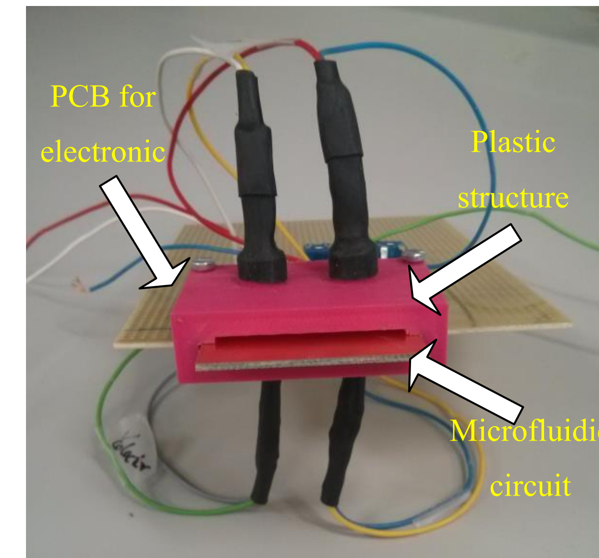

Fig.2. Complete setup

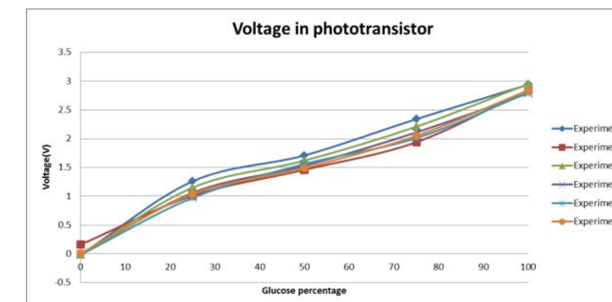

Fig.3. Voltage vs glucose for 1 cm light path cuvette

No liquid	Reagent liquid	100 mg/dl glucose
V=2 mV	V=13 mV	V=153 mV

Table.1. Experimental results for the proposed setup

Implementation of numerical methods for nanoscaled semiconductor device simulation using OpenCL

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***Abstract*—The present work implements solvers with OpenCL of the FGMRES and preconditioned BCGSTAB algorithms. These solvers are integrated in a 3-D simulation tool of nanoscaled MOSFET transistors. Simulations are launched in two different platform devices: NVIDIA Tesla S2050 and Intel Xeon Phi 3120A. The resulting times of execution are compared against the optimized PSPARSLIB version of the FGMRES solver. The results showed that a large computational charge compensate the overhead due to the data transfer time.**

I. Introduction

With the seizure in October 2010 of the leading position among the world's best performing supercomputers on the top500 [1] by the Tianhe-1A, constructed by China's National Supercomputing Center in Tianjin, the use of graphics processing units (GPUs) for general purpose computations became key to high performance computing. The emerging of new architectures, such as the Intel Xeon Phi family of coprocessors [2], demands for the implementation of parallel versions of algorithms on a multiplatform level.

Following that philosophy, the present work was devoted to develop parallel versions of linear solvers that could be executed on multiplatform systems. These linear solvers have been implemented and tested in a 3D finite-element (FE) simulation tool for nanoscaled semiconductor devices [3].

The aggressive scaling of MOSFET transistors in the nanometer regime and the use of new architectures and materials makes necessary the development of accurate and efficient simulation codes [4]. It uses the Drift-Diffusion (DD) model for the carrier transport and the Density-Gradient (DG) approach to include quantum corrections. The 3-D FE DD-DG simulator tool can also be applied to study of several semiconductor devices like : bipolar devices [5], HEMTS [6] and Solar Cells [7].

There are two programming models to write code for GPUs. The NVIDIA's CUDA and the Khronos' OpenCL. The main disadvantage of CUDA is that is designed to work on NVIDIA's GPUs only. On the other hand OpenCL offers the versatility of an open language truly for multiplatform systems. In the present work, OpenCL was selected by its portability and results were compared against the optimized PSPARSLIB library [8] due to its known robustness.

The present work is organized as follows: section II introduces the simulation tool, section III makes a brief introduction to OpenCL [9], section IV shows the algorithms and explains where the modifications were introduced, section V shows the tests done and the results gathered and finally, in section VI the conclusions of the present work are listed.

II. Simulation process

To describe the simulation process we start with the equations that compose the physical model. The Drift-Diffusion model with the Density-Gradient approach are described in the equations (1)-(5), where: equation (1) is Poisson's equation, equations (2)-(3) are the density gradient equations and equations (4)-(5) are the current density equations for electrons and holes:

$$\mathrm{div}(\epsilon\nabla\phi) = q(p - n + N_D^+ + N_A^-) \quad (1)$$

$$2b_n\frac{\nabla^2\sqrt{n}}{\sqrt{n}} = \phi_n - \phi + \frac{k_BT}{q}\ln\left(\frac{n}{n_i}\right) \quad (2)$$

$$2b_p\frac{\nabla^2\sqrt{p}}{\sqrt{p}} = \phi - \phi_p + \frac{k_BT}{q}\ln\left(\frac{p}{p_i}\right) \quad (3)$$

$$\mathrm{div}(J_n) = qR \quad (4)$$

$$\mathrm{div}(J_p) = -qR \quad (5)$$

with variables on the equations having their usual meaning [3].

The simulation process is as follows: once the mathematical model is fixed, the equations are discretized via the the Finite Element Method, this discretization is described in [3] with detail. Due to the nature of the mathematical model, non linear systems are generated which are then linearized by the Newton method. Then the resulting linear systems are solved. Finally the numerical results are obtained for its display and analysis. In Fig. 1 the simulation flow is shown.

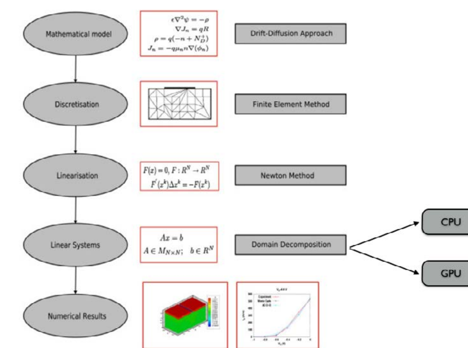

Fig. 1: Flow of the simulation process.

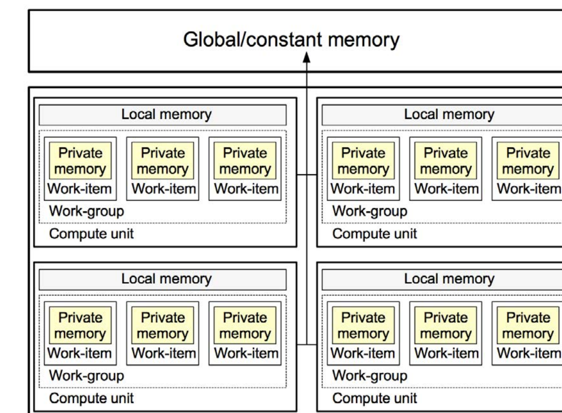

Fig. 3: OpenCL device model.

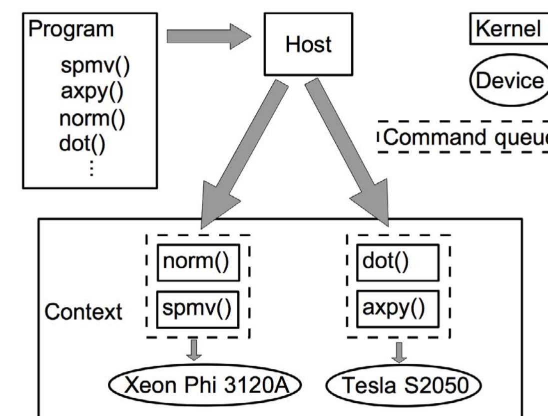

Fig. 2: OpenCL frame.

III. OpenCL

A. Frame

OpenCL enables parallel programming, which assigns computational tasks to several processing elements at the same time. In OpenCL notation these tasks are called *kernels*. A kernel is a special coded function to be executed by one or more OpenCL complaint *devices*. The devices where the kernels are executed can be GPUs, coprocessors or even the same CPU where the host application is running. The kernels are sent to the devices by a *host application*, which is a regular application executed on the user operating system. The host manages the connected devices using a container called a *context*. To execute the kernels on a specific device, first these must be sent to the device itself, in order to do it the host dispatch them via a *command queue*. A command queue is how the host comunicate kernels/commands to the device. The container where the kernels are searched by the host is called *program*. In Fig. 2 the interactions between the host, devices, context, programs, and kernels can be appreciated [9].

B. Device model

It is important to know the memory address spaces accesed by OpenCL; therefore, the device model of OpenCL is introduced. A device like a GPU card has several processing cores, known as *compute units*. A compute unit is capable of supporting a *work-group*, which is a set of *work-items* that access the same processing resources (e.g. local memory). Finally, a *work-item* is an individual kernel execution with a set of data. The OpenCL device model identifies four address spaces:

- *Global memory*: write/read memory that stores data for the entire device.
- *Constant memory*: read memory that stores data for the entire device.
- *Local memory*: stores data for work-items in a work-group.
- *Private memory*: stores data for a single work-item.

In Fig. 3 the relations between the diffent types of memory and the work-items, work-groups and compute units are shown.

When a host application sends data to the device, the data is stored in the global/constant memory. When the host reads data from the device, the data comes from the device global/constant memory. The global memory is the largest memory region, but it is also the slowest for work-items to access. The Local memory is accessed much faster than the global memory, but it is not as large as the global memory, so it is a good place to store intermediate results. Finally, the private memory is the fastest and smallest memory region, but due to its size it is important not to use much of it [9].

C. Technical specifications

From subsection III-B is deduced the importance of working with the local memory whenever is possible. However, there are differences between traditional GPUs and the Intel Xeon Phi coprocessors that affect the code programming. In the present work two devices were selected to work with: The NVIDIA Tesla S2050 [10] and the Intel Xeon Phi coprocessor 3120A [11].

The NVIDIA Tesla S2050 is based on the Fermi architecture. It enables the use of shared local memory between work-items in the same work-group. OpenCL enables manual

TABLE I: Technical specifications.

	Tesla S2050	Xeon Phi 3120A
Cores	448	57
Core clock (GHz)	1.10	1.55
Total memory (GB)	3	6
Memory max bandwidth (GB/s)	148	240
TDP (W)	225	300

ALGORITHM I: **FGMRES**

1. Compute $r_0 = b - Ax_0$, $\beta = ||r_0||_2$ and $v_1 = \frac{r_0}{beta}$
2. **For** $j = 1, ..., m$ **do1**:
3. Compute $z_j = M_j^{-1} v_j$
4. Compute $w = Az_j$
5. **For** $i = 1, ..., j$ **do2**:
6. $h_{i,j} = (w, v_i)$
7. $w = w - h_{i,j} v_i$
8. **End do2**
9. Compute $h_{j+1,j} = ||w||_2$ and $v_{j+1} = \frac{w}{h_{j+1,j}}$
10. Define $Z_m = [z_1, ..., z_m]$, $\bar{H}_m = \{h_{i,j}\} i \in [1, j], j \in [1, m]$
11. **End do1**
12. Compute $y_m = argmin_y ||\beta e_1 - \bar{H}_m y||_2$ and $x_m = x_0 - Z_m y$
13. **If** satisfied **stop**, **else** $x_0 \leftarrow x_m$ and GOTO 1 **End If**

control over the shared local memory in order to optimize the kernels running time. On the other hand, Intel Xeon Phi coprocessor 3120A includes a two-level cache system similar to most modern CPUs. Therefore, using the OpenCL shared local memory provides no benefit on the Intel Xeon Phi coprocessor. Furthermore, it introduces additional overhead in terms of redundant data copy and management. As mentioned before, this directly impacts on the way of coding the kernels from one platform to another, however, once the kernels are ready for each platform, the host application does suffer minor modifications or none at all, allowing a multiplatform code with minimum changes. In TABLE I the specifications of the devices used in the present work are shown.

IV. Solvers implementation

Two linear system solvers have been chosen to be implemented with OpenCL: the flexible variant of the GMRES method ALGORITHM I [8] and the preconditioned BCGSTAB method ALGORITHM II [12].

Both methods have already been tested in the simulation tool [13]. The preconditioner matrix is calculated by the incomplete LU factorization [8]. The selection of which version of the solver is to be executed, is made at execution time in the stage Domain Decomposition see Fig. 1; therefore the solver can be executed on GPU or CPU as selected.

We have identified the operations that both algorithms have in common: the dot product operation, the norm operation, the sparse matrix-vector product operation and the vector addition operation. On such operations was focused the effort of parallelizing with OpenCL. For example in step 1 of both algorithms the sparse matrix-vector product and the vectors addition operations are required. However, it is important to remark that not all the operations that could be parallelized, were parallelized. For example, the step 12 of the FGMRES requires computing the solution of an overdetermined system,

ALGORITHM II: **Preconditioned BCGSTB**

1. Compute $r_0 = b - Ax_0$
2. Choose $\hat{r}$, for example $\hat{r} = r_0$
3. **For** $i = 1, ...,$MaxIte **do1**:
4. $\rho_{i-1} = (\hat{r}, r_{i-1})$
5. **If** $\rho_{i-1} = 0$ method fails **End if**
6. **If** $i = 1$
7. $p_i = r_{i-1}$
8. **Else**
9. $\beta_{i-1} = \left(\frac{\rho_{i-1}}{\rho_{i-2}}\right)\left(\frac{\alpha_{i-1}}{\omega_{i-1}}\right)$
10. $p_i = r_{i-1} + \beta_{i-1}(p_{i-1} - \omega_{i-1} v_{i-1})$
11. **End if**
12. Compute $\hat{p} = M^{-1} p_i$
13. $v_i = A\hat{p}$
14. $\alpha_i = \frac{\rho_{i-1}}{(\hat{r}, v_i)}$
15. $s = r_{i-1} - \alpha_i v_i$
16. **If** $||s||$ satisfactory then $x_i = x_{i-1} + \alpha_i \hat{p}$ and stop **End if**
17. Compute $\hat{s} = M^{-1} s$
18. $t = A\hat{s}$
19. $\omega_i = \frac{(t,s)}{(t,t)}$
20. $x_i = x_{i-1} + \alpha_i \hat{p} + \omega_i \hat{s}$
21. $r_i = s - \omega_i t$
22. **If** $||r||$ satisfactory stop **Else** continue with $\omega_i \neq 0$ **End if**

22\. **End do1**

this is accomplished using the least-squares approach, but the order of magnitude of such systems does not compensate the overhead of transferring data to the device instead of executing the operation on the CPU itself.

V. Tests and results

The simulations were executed using three different mesh sizes. The smallest mesh (E001) has 11,931 nodes, the medium mesh (E002) has 121,316 nodes, and the largest one (E003) has 279,255 nodes. For each system solved the following metrics were collected:

- **iterations**: number of iterations needed for the solver.
- **residual norm**: the norm of the residual.
- **runtime solver**: time spent in the execution of the solver.
- **runtime pre-algorithm**: time spent in operations to set the frame where kernels can be executed, (eg. the association of kernels. with arguments made by the host before send them via a command queue [9]).
- **runtime algorithm**: time spent in operations like transferring arrays between host and device and executing kernels.
- **time transfers**: time spent transferring data between host and device.
- **time device**: time spent on kernel's executions.

In TABLE II a comparison between the two versions of the FGMRES solver is shown to ilustrate the metrics (the preconditioned BCGSTAB solver was not showed because it not contributed new information to the illustration). As can be appreciated, besides its the same algorithm the number of iterations to converge is different, the difference could arise from step 12 of ALGORITHM I. Also, it is appreciated the difference in the **runtime solver** metric. The OpenCL version of the algorithm is approximately 25 times slower than the PSPARSLIB version using the mesh E001. Clearly,

TABLE II: Information collected from solvers execution.

Xeon Phi 3120A	FGMRES	
E001	PSPARSLIB	OpenCL
iterations	2	4
residual norm	1.2371e-04	2.3601e-06
runtime solver	0.0084	0.2102
runtime pre algorithm (s)	N/A	0.0138
runtime algorithm (s)	N/A	0.1964
time transfers (s)	N/A	0.1002
time device (s)	N/A	0.0165

TABLE III: Tesla S2050.

Solver	Mesh		
	E001	E002	E003
FGMRES PSPARSLIB	363 s	6,309 s	32,607 s
FGMRES OpenCL	388 s	6,548 s	33,925 s
Preconditioned BCGSTAB OpenCL	423 s	7,162 s	34,740 s

TABLE IV: Xeon Phi coprocessor 3120A.

Solver	Mesh		
	E001	E002	E003
FGMRES PSPARSLIB	317 s	5,265 s	25,272 s
FGMRES OpenCL	368 s	5,571 s	26,222 s
Preconditioned BCGSTAB OpenCL	384 s	6,004 s	28,205 s

the overhead due to **runtime algorithm** and **time transfers** is taking its toll, just **time transfers** alone represents the 47% of the **runtime solver**. No attempt was done to optimize kernels, because as can be appreciated in TABLE II the **time device** represents the 7% of the **runtime solver**. To compensate the effect of **time transfers** on **runtime solver** larger meshes were used, see TABLES III and IV for results.

In Fig. 4 a comparison is made between the two OpenCL's version of the algorithm against the optimized PSPARSLIB version of FGMRES running with one process, the cases are as follows: Case 1: FGMRES PSPARSLIB vs. FGMRES OpenCL on Tesla, Case 2: FGMRES PSPARSLIB vs. Preconditioned BCGSTAB OpenCL on Tesla, Case 3: FGMRES PSPARSLIB vs. FGMRES OpenCL on Xeon Phi and Case 4: FGMRES PSPARSLIB vs. Preconditioned BCGSTAB OpenCL on Xeon Phi.

As can be appreciated in the Fig. 4, as the numbers of nodes increases the time difference against the optimized PSPARSLIB version decreases. The computational charge on the devices is gradually compensating the overhead due to **time transfers**.

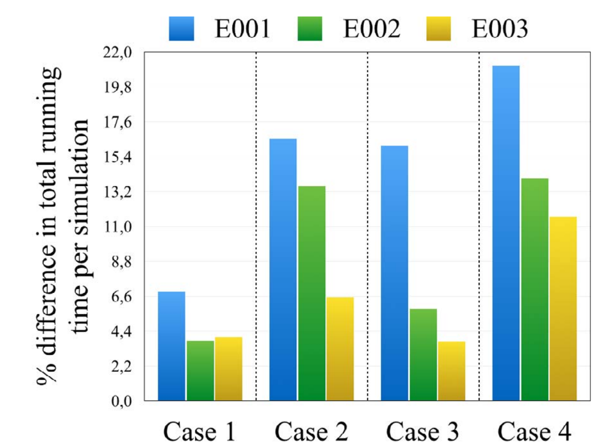

Fig. 4: Behaviour of solver with diffent sized meshes.

VI. Conclusions

The implementation of the OpenCL versions of the solvers was done correctly. As expected, the results showed that a larger charge on computational resources compensated the overhead due to data transmission from host to device and viceversa. The OpenCL versions of the solvers remained slower than the PSPARSLIB version up to the mesh of 279,255 nodes.

Acknowledgment

This work has been supported by FEDER funds and Xunta de Galicia under contract GRC 2014/008, and by Spanish Government (MCYT) under project TEC2010-17320 and TIN-2013-41129-P. N.S. has a Marie-Curie Fellowship under Grant PIEF-GA-2011-299990.

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Dry etching of graphene: from nanodots to microwires.

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1. Abstract

The expectations on graphene possible applications have increased dramatically since the discovery of its electrical properties in 2004.[1] These possible applications face obstacles from the industry point of view, such as graphene quality, compatibility and process integration issues. Commercialization of graphene and related 2D materials based devices requires the development of robust fabrication techniques for large scale etching in a device-fabrication facility. In this context, this contribution tackles the challenging problem of low-cost-patterning in graphene research. In this work, we discuss the effect on graphene of electrical micro discharges at different low DC voltages and applied probe forces using of a spring-probe with spring constant of 300 N/m±20%. We analyze the erosion process by means of micro Raman and AFM. According to the obtained the results, this electro-erosion based etching procedure [2] is proposed as scalable to large area (cm^2), economical green technology for structuring graphene films on any substrate. The possible mechanisms involved in the patterning processes are discussed. It is shown that under the appropriate conditions, we can obtain from high quality nanographene, with size around 18 nm (Fig.1), to graphene micro-ribbon lattices whose dimensions are down to 1 µm in width and millimeters in length (Fig.2), very promising for terahertz graphene plasmonic applications.

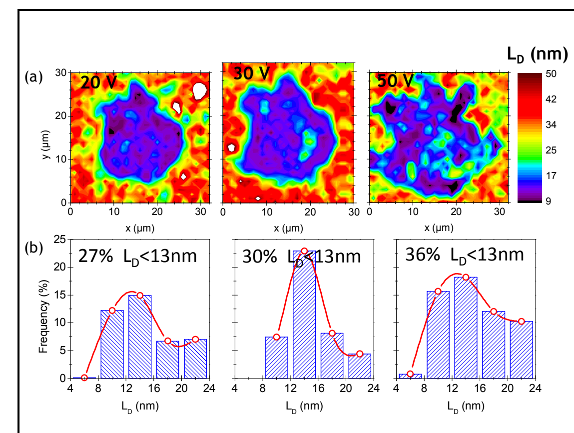

Fig.1. L_D Raman maps (a), and the corresponding size distribution for the eroded areas (b).

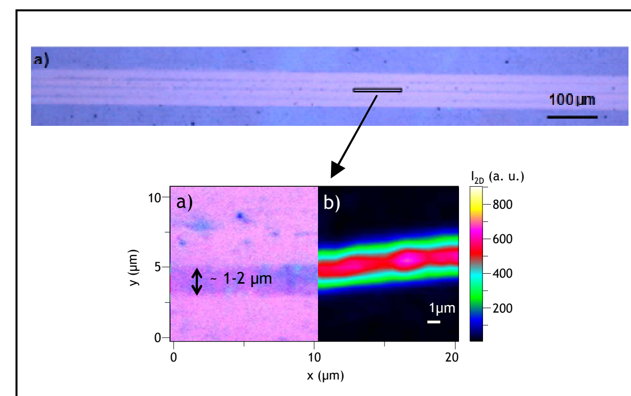

Fig.2. a) Optical image of graphene micro-ribbons (1 µm × 1200 µm) and (b) I_{2D} Raman image corresponding to the rectangular marked area.

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Liquid-crystalline pushing micropillars as actuators for haptic devices

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1. Abstract

A novel liquid-crystalline elastomer-based micropillar array with pushing properties is obtained by the combination of the two step crosslinking strategy and a molding process, together with the application of uniaxial compression before the final curing. Thus, the micropillars are oriented resulting in a novel 2D prolate polydomain conformation of the material, opening new opportunities for their integration as actuators in microsystems.

2. Introduction

The combination of the liquid crystal anisotropy and the entropy elasticity of polymer networks results in materials with unique physical properties: liquid-crystalline elastomers (LCEs), which produce reversible actuation under the application of external stimulus [1]. Thus, new generation of microactuators can be designed based on LCEs, combining material processing and microengineering [2,3]. Here we present a successful nematic side-chain LCE micropillar array based on siloxane chemistry which expands in the direction of the applied orientation when the isotropic temperature is reached [4]. This behavior, related to the conformation changes of the polymer backbone, allows for the obtaining of micropushers with actuation temperatures around 55 °C.

3. Results and discussion

In the nematic state, the LCE micropillars have average dimensions of 3.00 mm in height and 2.46 mm in diameter, dimensions which changed to 3.63 mm and 2.10 mm respectively after heating the LCE array to the isotropic phase (**Fig.1**), resulting in an expansion factor of ez = 21% along the axial direction and a contraction factor of e r = 15% in the radial direction upon isotropization of the sample. The mechanical actuation was analyzed by measuring the forces exerted by the micropillars during either expansion upon heating and contraction upon cooling as function of time, by using an accurate dynamometer and a custom-made Peltier element. **Fig.2** show a complete heating-cooling cycle for four different micropillars measured under the same conditions. The maximum measured force was F = 20 mN (5.6 kPa of equivalent stress) at the set temperature of T = 90 ºC, leading to a change in height of Δz = 630 µm) for an actuation time of about t = 110 s. Same measurements were repeated for several cycles, showing a reproducible and fully reversible behavior.
In parallel, swelling, X-ray and calorimetry experiments were performed confirming the novel 2D prolate polydomain conformation of the LCE material.

4. Conclusion

A new LCE micropillar array of pushing actuators with 2D prolate polydomain conformation has been successfully synthesized by the combination of uniaxial compression and molding, reaching actuation around 55 ºC with measured forces up to 20 mN. These values, together with the processability and tunability of the chemistry in terms of mechanical and thermal actuation, and the possibility of obtaining different shapes on demand – besides the common LCE strip –, make these LCE actuators very suitable candidates for haptic applications, as well as for their integration in Microsystem Technology, in the development of complex devices through batch processes.

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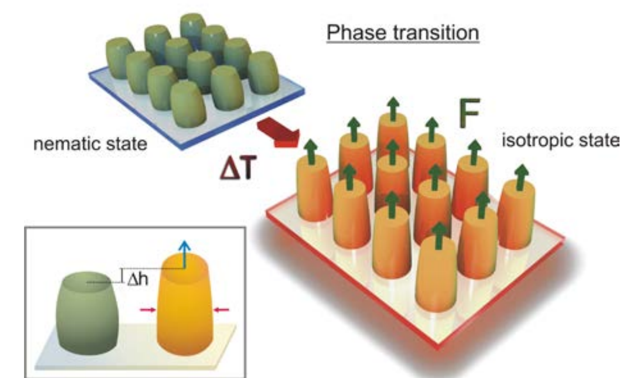

Fig.1. Scheme of the LCE micropillar actuators with pushing properties obtained by uniaxial compression. The temperature to promote the phase transition and thus, actuation is around 55 ºC.

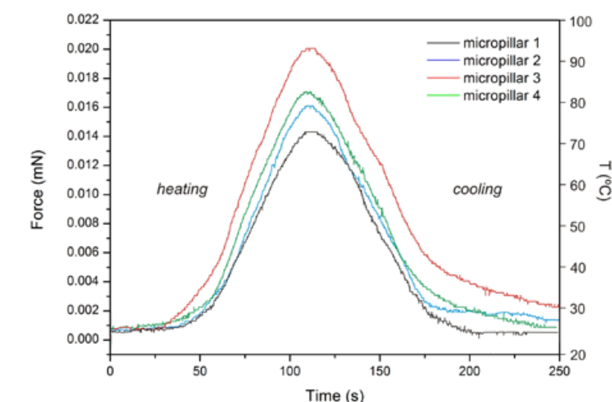

Fig.2. Thermo-mechanical response of four different micropillars as function of temperature and response time.

All-inkjet printed organic transistors: Strategies to minimize variability

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Abstract

Ink-jet printing is a desirable manufacturing technique for low-cost, large-area and flexible organic electronic circuits. This fabrication method uses a small amount of materials, it is a mask-less additive method and well-suited for applications that require heterogeneous integration of different materials and functional devices on the same substrate. However, Ink-jet printing is also highly susceptible to process variation leading to a variability on the organic thin film transistor (OTFT) parameters.
Variations between OTFTs had been a well-known problem more acute than in silicon-based technologies by an inherently much higher parameter spread. Reasons for that, include, irregular morphology of the semiconductor, difficulty in controlling the precise dimensions of OTFTs, mobile trapped charges in the dielectric, uneven material deposition, roughness of the semiconductor-gate dielectric interface which leads to mobility variations between the different transistors.
The large transistor variability poses a serious challenge to the cost-effective utilization of organic circuits. Meeting this challenge requires comprehensive and efficient approaches for variability characterization and minimization. Accurate and efficient characterization of the different types of variation requires a large number of measurements on a variety of devices, layout styles, and environments.
Other groups previously reported data on transistor variability; Wei Xiong [1] concluded that the variability observed prohibits the use of their OFETs in configurations that rely on precisely matched currents, as for instance current-steering D/A converters. The IMEC group has recently reported that the methodology used in CMOS technologies to account for local parameter variations and transistor mismatch can be transposed to organic thin-film transistor technologies [2].
In this contribution we address the sources of variability in inkjet printed OTFTs. Intrinsic sources of variation caused by materials, processing and by bad transistor design are presented and discussed.
Variability on the OTFTs parameters (mobility, on-off/ratio, the threshold voltage) can be introduced by the wetting properties of the inks used. Phenomena like the Marangoni or the coffee stain effect cause that the printed layer thickness does not scale with the printed area. These effects are assessed using capacitance-voltage measurements and by morphological characterization techniques.
Parasitic effects such as a lateral surface conduction, fringing currents and large off-state currents also introduce variability on the TFT parameters. We discuss how these effects can be easily identified from the electrical characteristics, moreover we present how it is possible be minimized or even eliminated these parasitic by using appropriated OTFT layout.
This work received financial support from European Community Seventh Framework Programme through the project “Technology Design Kit For Printed Electronics (TDK4PE).

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Synthesis of PbS/Semiconducting Polymer Nanocomposites Via Thiolate Decomposition

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1. Abstract

In this work we present a simple method to obtain a hybrid polymer-nanoparticle composite by decomposition of nanoparticle precursors, either in an organic solvent or directly in a semiconducting polymer solution. The study has been carried out employing typical materials for photovoltaic applications, like poly(3-hexylthiopene-2,5-diyl) semiconducting polymer and PbS nanoparticles. However, the method may be easily extended to other organic polymers and nanoparticles.

2. Introduction

Hybrid nanocomposites consisting of conducting conjugated polymers and semiconductor nanocrystals combine the advantages of both materials. Organic polymers are low-cost materials which are easy to process from solution by means of an affordable technology. Semiconductor nanocrystals possess unusual properties conferred by the strong quantum confinement, such as tunable light absorption and emission, and multiple exciton generation. Many efforts have been devoted to the synthesis of composites in order to be used as the active material in devices such as organic light emitting diodes or solar cells.

3. Experimental

The synthetic route used to obtain PbS nanoparticles capped with decanothiol consists of two steps: (i) reaction of decanothiol and a lead salt to produce metal decanothiolate [1], which is subsequently washed and centrifuged, and contains both metal and capping radicals; and (ii) decomposition of the thiolate dissolved in chlorobenzene which result in the formation of semiconductor nanoparticles [2]. The thiolate decomposition is assisted via the addition of elemental sulphur. Nanoparticles may either be added in a later stage to a solution polymer or synthesized directly in the polymer solution. In the former case, only the decanothiol organic radical contributes to the stabilization of the nanoparticles. If the reaction takes place in the polymeric solution, both the organic radical and the polymer may stabilize de nanoparticles. The resulting composites have been analyzed by Transmission Electron Microscopy (TEM), thermogravimetry and UV-VIS absorption spectroscopy.

4. Results

Thermogravimetry mesurements show that lead thiloate decomposition takes place at 288ºC. However, the addition of elemental sulfur promotes the formation of nanoparticles at room temperature. TEM observations (fig. 1) show that the resulting nanoparticles embedded in P3HT have uniform dispersion and an approximate average size of 6 nm. The nanoparticle solution shows increasing optical absorption as the sulfur /Pb thiolate ratio is raised from 0% to 70%. Thus, potential photovoltaic devices based on P3HT may benefit of the addition of PbS nanoparticles since the optical absorption of the polymer in the visible range may be extended by the addition of the nanoparticles. Besides, the optical absorption edge related to the nanoparticles is found to be far above the value of bulk material, which indicates that strong quantum confinement has been achieved. The addition of elemental sulfur to the metal thiolate solution results in higher density of nanoparticles due to the assisted thiolate decomposition.

5. Conclusion

A simple method to synthesize nanocomposites based on metallic sulfur nanoparticles and semiconducting polymers has been presented. The chemical route allows the synthesis of the nanoparticles directly in a polymer solution avoiding residuals in the resulting material.

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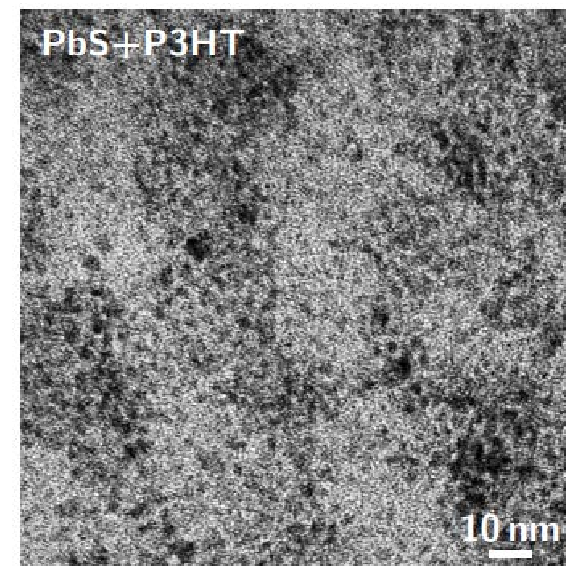

Fig.1. TEM image of PbS nanoparticles embedded in P3HT polymer

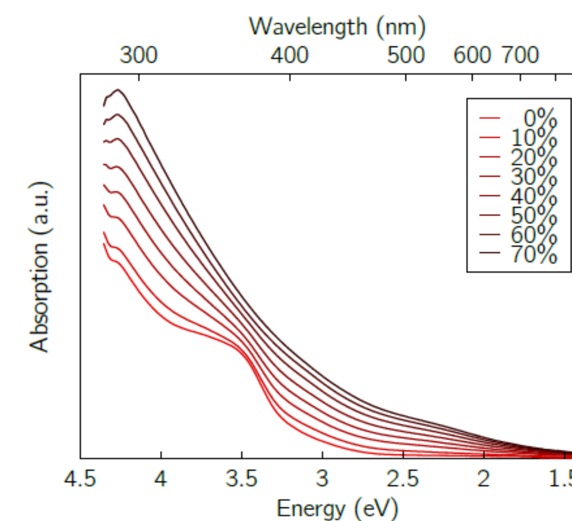

Fig.2. Optical absorption of PbS nanoparticles with sulfur/Pb thiolate mole ratio increasing from 0% to 70%

Electrostatics and drift-diffusion current model of bilayer graphene field-effect transistors

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1. Abstract

Bilayer graphene exhibits the remarkable property of energy gap tunability with the perpendicular electric field, so it has been suggested that it could be useful as active material for making transistors targeting both digital and analog/radio frequency (RF) applications. In this work, a physics-based model for the drain current of dual gate bilayer graphene field-effect transistors (BLGFETs), suitable for exploring the design parameter space, is developed. The appropriate band structure and 2D density-of-states of the bilayer graphene has been taken into account to deal with the BLGFET electrostatics. Then, a drift-diffusion mechanism for the carrier transport through the bilayer graphene has been considered, with the quantum capacitance playing a key role. The model has been benchmarked against prototype transistors reported in the literature and we present some figure of merits relevant in RF applications.

2. Introduction and results

The semiconductor industry has been facing an exponential growth of the number of transistors per chip during the last three decades. It is also desirable the gate length to be around 4.5 nm by 2023 following the International Technology Roadmap for Semiconductors (ITRS). However, maintaining this trend is a major challenge for both the industry and scientific community due to arising short channel effects. As a result, new device structures have been proposed such as nanowire field-effect transistors (NWFET), multiple gate devices (MuGFETs, FinFETs), carbon nanotube field-effect transistors (CNTFETS), graphene nanoribbon field-effect transistors (GNRFETs) and mono- or multilayer graphene field-effect transistors (GFETs or MLGFETs). Among them, graphene based devices have attracted the attention of scientific community due to the prospect of ultrahigh carrier mobilities and saturation velocity exceeding those of the conventional semiconductors. This has motivated intensive work focused on the development of graphene metal-oxide-semiconductor field-effect transistors [1]. The gapless nature of single layer graphene, which is considered as the main obstacle on its application in graphene based electronics, causes the gate voltage to be unable to switch off the device and are not suited for logic applications. However, it still seems very promising for RF and analog applications because of the high transconductance and relatively low output conductance. Cut-off frequencies up to 427 GHz and maximum frequency of oscillation of 45 GHz has been demonstrated, which are important figures of merit in RF. Besides the metal-graphene contact resistance issue that strongly contribute to RF performance degradation, the lack of an energy gap is also a detrimental factor preventing a full saturation of the drain current. It was suggested, in order to get better saturation, replacing the single-layer graphene by bilayer graphene as the transistor channel [2]. In bilayer graphene a band gap can be induced by applying a potential difference between two layers as a result of a perpendicular electric field. That potential difference can be realized with an applied gate field, meaning the band gap can be controlled by gate bias [3]. In this work, we have developed a model of the electrostatics for the transistor sketched in Fig. 1. For these simulations we have taken device parameters from Ref. [4]. In doing so we have taken into account screening effects and the influence of trapped charges. Main results are shown in Fig. 2. Next, we have developed a drift-diffusion model for the transistor drain current. The model has been augmented considering contact effects as well. The model outcome compares pretty well with experimental results, confirming the superior saturation behavior (Fig. 3) together with a noticeable enhancement of the on/off current ratio (Fig. 4) as compared with monolayer graphene.

Acknowledgements

The research leading to these results has received funding from Ministerio of Economía y Competitividad of Spain under the project TEC2012-31330 and from the European Union Seventh Framework Programme under grant agreement n°604391 Graphene Flagship.

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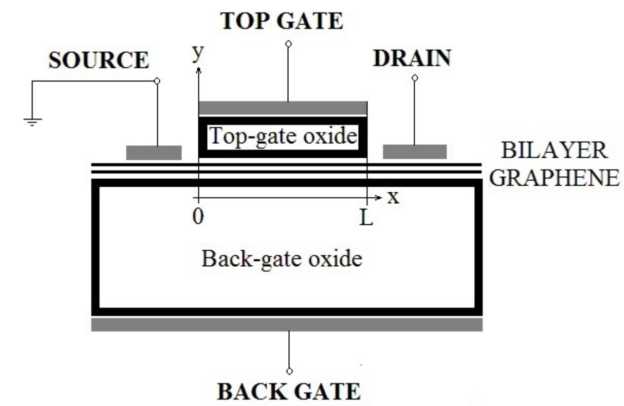

Fig. 1 Cross section of the bilayer graphene field effect transistor. It consists of two graphene sheets playing the role of the active channel. The electrostatic modulation of the carrier concentration in the 2D sheet is achieved via a double-gate stack consisting of top and bottom gate dielectrics and corresponding metal gates. The source is grounded and it was considered as the reference potential.

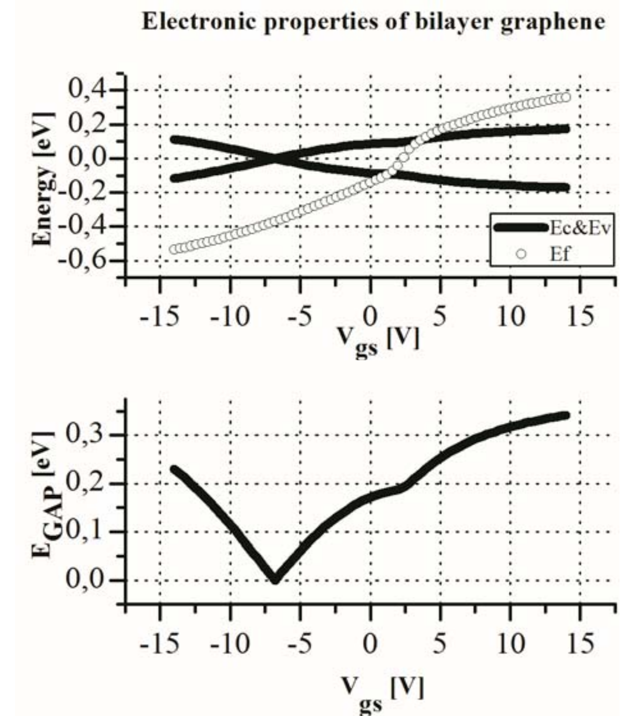

Fig. 2 Bilayer graphene energy diagrams of a BLGFET and for a fixed bottom gate bias V_{bs}=-60V (top and bottom oxide thicknesses t_t=8nm, t_b=90nm; and dielectric constants ε_t=3.9, ε_b=3.9; respectively, related to the device in Ref. [4]). Here, *Ec* and *Ev* are the conduction and valence band edge respectively; *Ef* is the Fermi level; E_{GAP} is the energy band gap; and V_{gs} is the top gate bias.

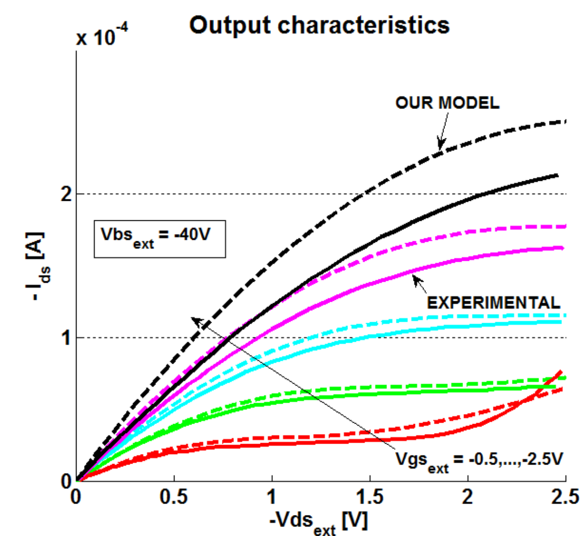

Fig. 3 Output characteristics of a double gate bilayer graphene field effect transistor and comparison with experimental data from Ref. [4].

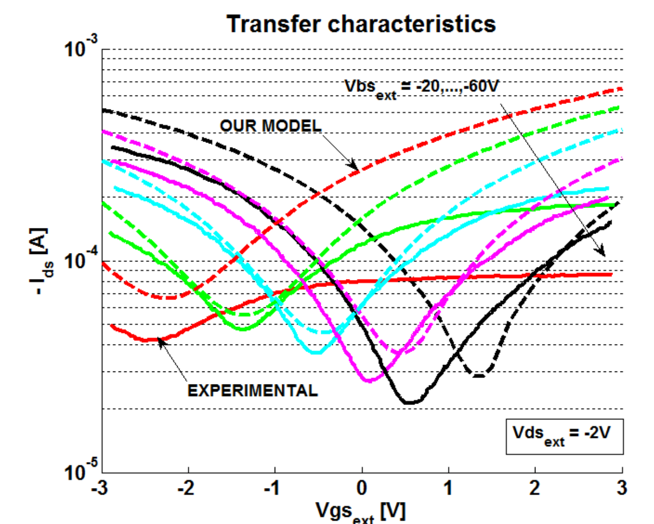

Fig. 4 Transfer characteristics of a double gate bilayer graphene field effect transistor and comparison with experimental data from Ref. [4].

Radiation Effects in nanometric SRAMs induced by 18 MeV Protons.

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1. Abstract

This paper presents experimental results of Soft errors caused by proton interactions in SRAM devices implemented with a 65nm CMOS technology using the 18 MeV proton facility at the National Center of Accelerators (CNA) in Seville.

2. Introduction

This work is centered in the analysis of the Soft errors in SRAM devices produced by the interaction of protons with the silicon substrate. It has been observed that the interaction of protons with the silicon lattice is capable to generate secondary particles, that in turn create the enough electric charge to change the logic state of a memory bitcell, causing a Single event upset (SEU).

3. Experiment

The circuit under test was a specific design containing three different memories implemented with a commercial 65nm CMOS technology. Accelerated test with proton irradiation was performed at the national center of accelerators (CNA) in Seville (Fig. 1).

The proton energy used was 18 MeV. In this way, the proton energy which hit the chip surface was about 17 MeV. To avoid an excessive degradation of circuit devices, the total ionization dose, D, was limited to 120 Krad [1]. D is given by:

$$D = K \cdot LET \cdot \emptyset \qquad \text{Eq1.}$$

Where K is a constant conversion factor (Table 1), LET is the linear energy transfer that describes the energy loss per unit path length of a particle as it passes through a given material (Table 1) and $\emptyset$ is the proton beam fluence in proton/cm^2. Therefore $\emptyset$ must be lower than $3{,}4\cdot10^{11}$p/cm^2 to satisfy the total ionization dose restriction. Beam fluence and flux $\emptyset_t$ were related by the irradiation time t_{rad}

$$\emptyset = t_{rad}\,\emptyset_t \qquad \text{Eq 2.}$$

Beam flux was difficult to maintain controlled under $1{,}6\cdot10^9$p/cm^{2}s, therefore the total irradiation time must be lower than 240 s. To carry out the experiment the memories were initialized to a known state, they were irradiated with a proton beam flux of $1{,}6\cdot10^9$p/cm^{2}s during 60 s, after that the memory content was read in order to detect single event upsets. This procedure was repeated two steps more until a total irradiation time of 180 s. was reached.

4. Results

Two chips were measured (fig 3 and 4); the first one was a fresh part while the second one was previously irradiated with alpha particles. Although the alphas have a small total dose irradiation, it is reasonable to suppose that the TID at the end will be different. Single event upsets were observed in both components, number of SEUs is reported in Tables 2 and 3.

5. Conclusions

The sensitivity respect to Total Ionizing Dose (TID) and Single-Event Upsets (SEUs) of a 65 nm CMOS technology with proton radiation has been obtained. Behaviour in both chips is very similar. The low number of detected events complicated the tolerance to radiation of the 3 different memories available in each circuit.

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Fig.1. FPGA and RS232 cable on robot arm front proton beam.

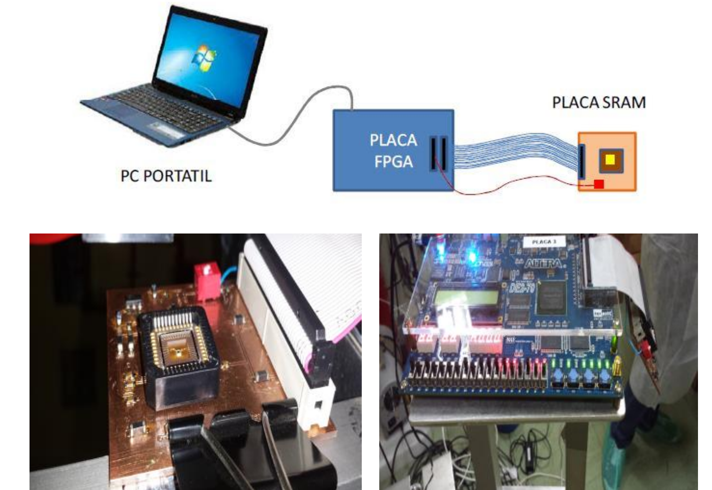

Fig.2. FPGA and PCB for control of the memory and communication with a computer.

Protons 17 MeV	
K	$1{,}602\cdot10^{-5}$ rad·mg/MeV
LET	0,022MeV·cm^2/mg

Table 1.

Chip1 Alphas + Protons	
ϕ_t	Number of events included in the file in the different memories: 1 − 2 − 3 (2048 bytes per row)
30Krad	No
60Krad	14 − 7 − 5 (row)
90Krad	26 − 10 − 8 (row)
120Krad	40 − 15 − 13(row)

Table 2. Results obtained in the chip 1.One event in a row means that at least there is one SEU in that period.

Chip2 Protons	
ϕ_t	Number of events included in the file in the different memories: 1 − 2 − 3 (2048 bytes per row)
30Krad	No
60Krad	No
90Krad	13 − 9 − 11(rows)
120Krad	22 − 18 − 26(rows)

Table 3. Results obtained in the chip 2.

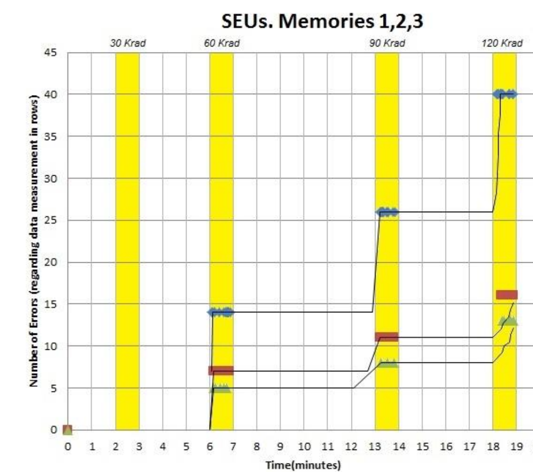

Fig3. Chip 1 data.

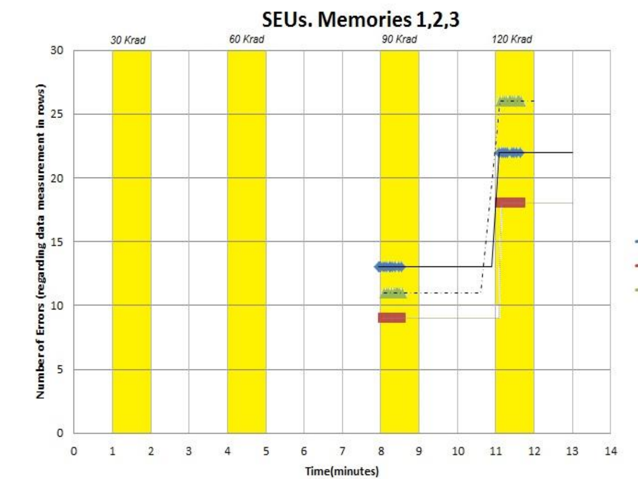

Fig4. Chip 2 data.

Time-dependent physics of double-tunnel junctions

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1. Introduction

The recent progresses in the fabrication of single-electron devices (SEDs) allowed the observation of well-defined Coulomb oscillations at room-temperature in single-electron transistors (SETs), paving the way of future applications [1]. Moreover, detection of single-electron events are now performed experimentally, giving access to current fluctuations [2], and in particular measurements of shot noise (SN), which gives more information on electronic transport than conductance and thus has been intensively studied over the last decades [3]. Most of the theoretical models for SN in SEDs are based on the full counting statistics tool (FCS) [4], calculating all zero-frequency current-correlations from probability distributions of number of electrons transferred during a long period of time. However, the frequency- and time-dependent physics of SN is less explored. On this purpose, a new method emerged recently, focusing on the distribution of time delays between two consecutive tunnel events in a barrier, also called waiting time distributions (WTDs) [5]. In this work, we use the homemade 3D self-consistent code SENS (Single-Electron Nanodevices Simulation) [6] to calculate and analyze WTDs and autocorrelation functions (AFs) of a Si quantum dot (QD)-based double-tunnel junction (DTJ), schematized in Fig. 1, at different biases.

2. SENS code

The first stage of the simulation relies on the calculation of the electronic structure of the QD according to the bias voltage and the number of electrons inside it by solving the Poisson-Schrödinger coupled equations within the Hartree and effective mass approximations.

The resulting wavefunctions are then used to compute the tunnel transfer rates source-to-dot Γ_{in} (N) and dot-to-drain Γ_{out} (N) depending on the number of electrons N in the QD by means of the Fermi golden rule and Bardeen formalism. Finally, the transfer rates are introduced in a Monte-Carlo algorithm to follow the time-evolution of the number of electrons in the dot, giving access to all electrical characteristics, such as current, WTDs and AFs. Analytical expressions have been derived for AFs and WTDs for the case of a maximum of 2 electrons in the QD that reproduce exactly the predictions from MC simulations.

3. Results and discussion

The simulated DTJ consists in a 8-nm-diameter Si-QD, with source and drain tunnel barriers of 1.2 nm and 1.8nm thicknesses, respectively. The current and Fano factor, F, are shown in Fig. 2. The current shows a positive differential conductance in the first two Coulomb stairs, while a negative differential conductance is observed in subsequent stairs. F decreases on the two first stairs, reaching its minimum just before the third step, and then increases until reaching its maximum at the beginning of the fourth step. The behaviour of the current and F are explained in previous articles [6, 7].

AFs and WTDs for three particular biases (minimum, maximum and Poissonian Fano factor) are given in Fig. 3. In the case V = 1.13 V, where F is maximum, the maximum of WTD occurs at the shortest times. The current pulses are thus positively correlated for low times and the AF shows positive values that vanish for times around 10^{-6} s, when the correlations are lost. Conversely, the WTDs show a maximum at intermediate times for the two other cases. This means that it is more unlikely to find another current pulse before this time-delay, and thus the AFs shows negative values at lower times. For delay times approaching the maximum of the WTD the probability of having current pulses with such delay times is increased, thus providing positive values of the AF. We have to remark that at long times the time dependence of AF and WTD are slightly different, as the WTDs concern only two consecutive current pulses, while the AFs correlate any tunnel events with another, not only consecutive ones. As a consequence AFs tend to vanish for longer times than WTDs.

If we are in the second step of the Coulomb staircase, only two electrons can enter in the QD. Thus, the only evolutions of the number of electrons in the dot which can provide current pulses are 0→1 (01) and 1→2 (12). To go deeper in the understanding of the origin of shot noise suppression/enhancement, we can separate the contributions of the different types of current pulses to the AFs. We have then plotted in Fig.4(a) auto- and cross-correlations of current pulses originated from (01) and (12) transitions for the bias with minimum F (V = 0.87 V). The corresponding WTDs are shown in Fig.4(b), separated in the 4 possible types of consecutive current pulses: two consecutive (01) and (12) pulses, (01) followed by (12) pulses, and inversely.

The positive values of the WTD at low times come from the contribution of the consecutive (01)-(12) events, whose maximum takes place at zero time (no other intermediate transition is necessary). On the other hand, negative values of the AF at low times are originated from the other 3 types of consecutive events, whose WTD has a maximum at a certain intermediate time delay (since 2→1, and/or 1→0, transitions are needed between two consecutive current pulses). They also generate positive correlations, but at the times where two current pulses are probable, in parallel to the maximum of the WTDs. Moreover, the weight of each of the contributions of the four different correlations is given by the amount of events of each type.

In Fig. 4, due to the values of the tunnel transfer rates (not shown here), the major contribution of current comes from (12) transitions (87 % of the total current). Then, the total AF essentially follows the behaviour of $C_{12\text{-}12}$, i.e. the AF of (12) pulses. $C_{12\text{-}12}$ is negative for low times and then increases with its corresponding WTD $W_{12\text{-}12}$ until reaching its maximum and finally decreasing to the uncorrelated value for long times.

The results for other bias points and more detailed explanations about the relationship between shot noise suppression/enhancement and the time dependence of the AFs and WTDs and the contributions of the different transitions will be presented at the conference.

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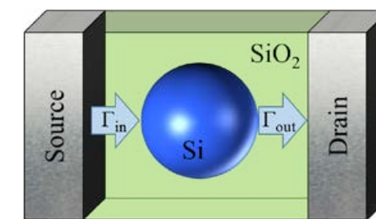

Fig.1. Schematic view of a DTJ.

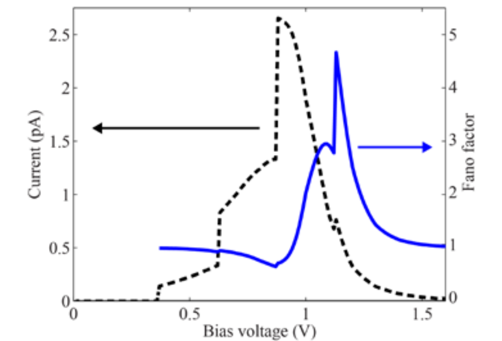

Fig.2. Current (dashed) and Fano factor (solid) as a function of the applied voltage.

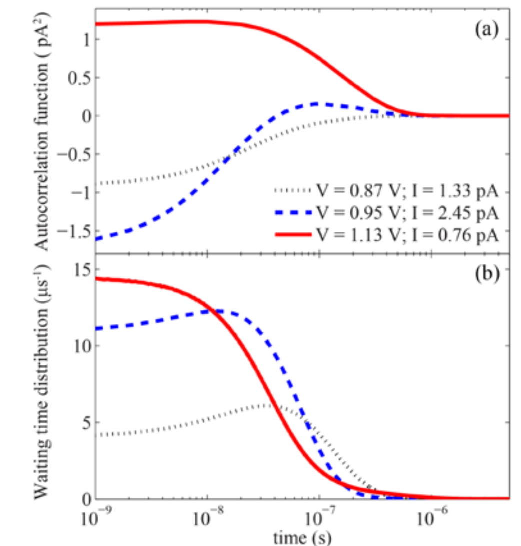

Fig.3. (a) AFs and (b) WTDs as a function of the delay time for 3 different biases corresponding to the minimum (V = 0.87 V), maximum (V = 1.13 V) and Poissonian (V = 0.95 V) values of the Fano factor.

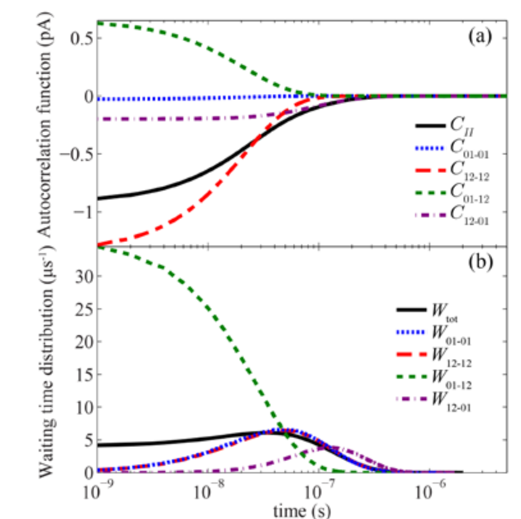

Fig.4. (a) Auto- and cross-correlation functions and (b) WTDs between (01) and (12) current pulses as a function of time, for a bias V=0.87 V corresponding to the minimum of F.

Geometrical effects on the quality factor of extensional microplate resonators in liquid

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Different reports [1, 2, 3] confirm the feasibility of miniaturized resonators for applications in liquid media. A step further to optimize the performance of these devices is the analysis of the fluid-structure interaction (FSI) [4]. Here we make use of a finite element method (FEM) model in order to obtain the optimum Q-factor of rectangular micro-plates that vibrate at the first extensional mode in liquid. The effect of both the length and the thickness of the plates were considered. The simulated results were compared with experiments in liquids of various viscosities. In addition, the model allowed us to design new taper-based structures with improved performance in viscous media.

Plates with different dimensions anchored in the middle of their length (see Fig. 1a) were characterized electrically and optically in different fluids using an impedance analyzer and a speckle pattern-based interferometer. In addition, a 2D FEM model (see Fig. 1b) was developed using the software ADINA. Fig. 2 shows the results from these simulations along with experimental data and reveals that our simulated Q-factors are much closer to the experimental results than the analytical approximation [5] in both tendency and absolute value. Moreover, the simulation predicts a maximum in the quality factor for a given length that can also be observed in the experimental results. Values of Q above 60 were measured in isopropanol.

It is highly remarkable that for a given thickness, there is a critical length which maximizes the quality factor, as it is shown in Fig. 3. Besides, the thicker, the higher the maximum Q-factor, as well as the corresponding critical length.

More detailed information about the losses can be drawn from the FEM model following a similar procedure as in [4]. The distribution of losses around the structure suggested the potential benefit of a tapered geometry like the one in Fig. 4, where the area with higher harmonic speed is decreased with respect to the rectangular plate. Tapered structures with the same top area but different taper angle, from rectangle to rhombus, were designed, fabricated and characterized (see Fig. 4). Fig. 5 shows the quality factors obtained in the characterization of these structures and the results from the 2D simulations.

Despite the fact that the solid in the 2D model consists of an XY-plane sectional area of the tapered plate, the 2D model keeps the trend between the quality factor and the taper angle and confirms that the rhombus resonator has almost twice the quality factor of a rectangular plate for the same top area and thickness.

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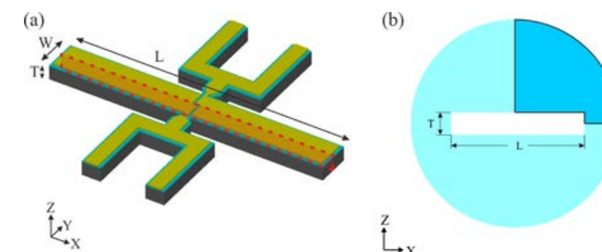

Fig.1. (a) 3D representation of the plate structures for the length-extensional mode study. The plates are anchored in the middle of its length using a T-shape structure to reduce the support losses. The red dashed area represents the 2D cut used in the FEM modelling. (b) Schematic representation of the 2D FEM model. Due to the symmetry of the problem, the fluid region can be reduced to the darker area.

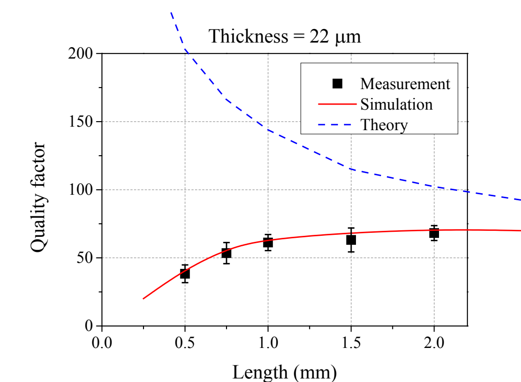

Fig.2. Q-factor of the extensional mode for different plates in isopropanol. The experimental measurements come from the electrical impedance characterization, the FEM simulations were performed over a 2D model and the theoretical results were obtained using the expressions given in Ref. 5.

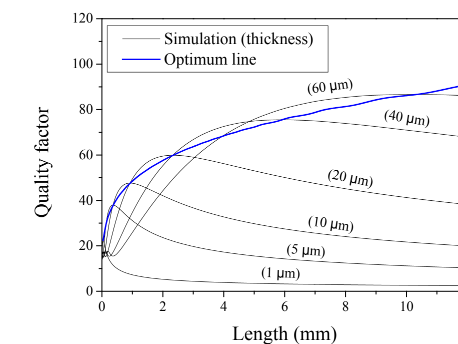

Fig.3. Quality factors from the simulation model for different lengths and thicknesses in isopropanol. The thicknesses are indicated over each line. The blue line represents the highest quality factor achievable for a given length.

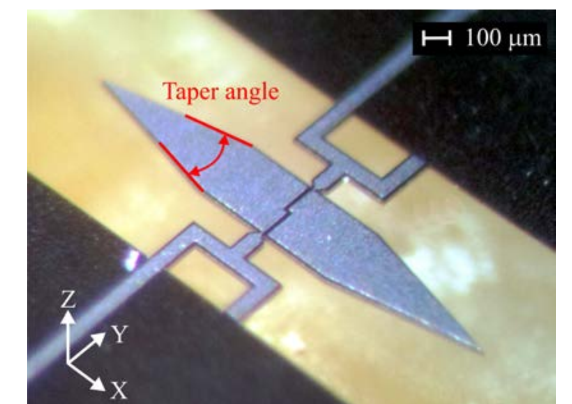

Fig.4. Optical micrograph of a fabricated tapered microplate with top area of 1000x250 μm^2 and taper angle of 27º. Brighter zones represent the Al electrodes.

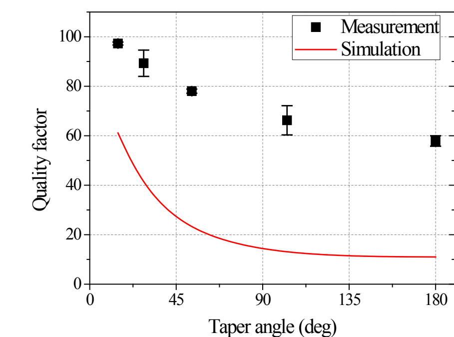

Fig.5. Measured and simulated quality factors in water for tapered micro-plates with a top area of 1000x250 μm^2 versus the taper angle.

Spectral Coupling of Atmosphere and the Performance of Perovskite Solar Cells

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1. Abstract

Third generation PV devices [1] offer cheaper manufacturing processes compared to current PV technologies. Among these devices, dye sensitised solar cells (DSSC) and perovskite solar cells have attracted the interest of scientific community due to their conversion efficiencies [2]. Fig.1 shows the efficiency chart for emerging thin film and new generation solar cells.
The study of different materials to replace the liquid electrolytes in dye-sensitised solar cells (DSSC) has led to the development of perovskite structured semiconductors based solar cells [1]. The perovskite solar cells usually follow three different architectures as shown in Fig. 2 in order to achieve higher efficiency and increase the robustness. Furthermore, the efficiency of these types of solar cells is impressive in the laboratory with a current conversion efficiency of more than 19%, Fig. 1 [2].
Under real operating conditions, the performance of solar cells is strongly affected by the time-varying atmospheric parameters. PV devices are spectrally selected and its behaviour is affected by the changes of the spectral distribution. In particular, air mass (AM), aerosol optical depth (AOD) and precipitable water (w) have demonstrated to be the parameters with the highest impact [3]. Recently, the analysis of the effect of the incident spectrum on the performance of different photovoltaic devices such as single-junction and multi-junction PVs has been addressed by several authors. However, the study of spectral changes on the performance of perovskite solar cells has not been analysed and is still unknown. This is a crucial task from the industrial perspective of perovskite solar cells.
This work focuses on the analysis of the influence of the time varying solar irradiance spectrum on the performance of perovskite solar cells.
In order to address this issue, the same approach introduced by the authors for understanding the performance of concentrator photovoltaic devices based on different optics and multi-junction cells is used [4]. This article aims to analyse the individual impact of atmospheric parameters (AM, AOD, w) for better understanding of the perovskite solar cells performance in different atmospheric conditions. Fig. 3 shows the effect of air mass on the perovskite solar cells performance. The influence of the spectral variations on the performance of perovskite solar cells on an annual or monthly time scale at locations with different atmospheric conditions is crucial for a better understanding of the performance of perovskite solar cells and their potential under real operating conditions. Fig. 4 shows the annual impacts of the spectral variations on the performance of perovskite solar cells at the locations described in table 1.
A complete analysis of the effects of each atmospheric parameter and the annual/monthly impacts of spectral variations on perovskite solar cells will be reported. In addition, a comparison with other materials similar to perovskite solar cells from the commercial perspective such as CdTe and CIGS solar cell will be also provided.

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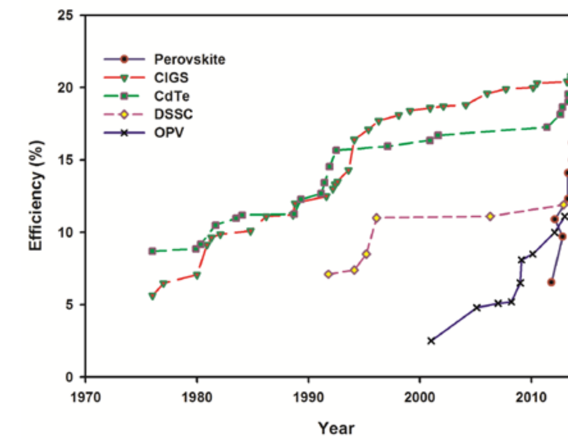

Fig.1. Efficiency chart for the emerging thin film and new generation solar cells.

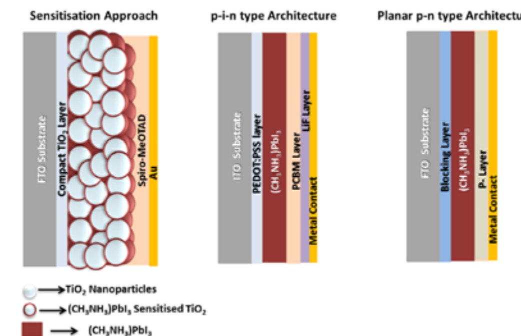

Fig.2. Common perovskite solar cells architectures reported in the literature to date.

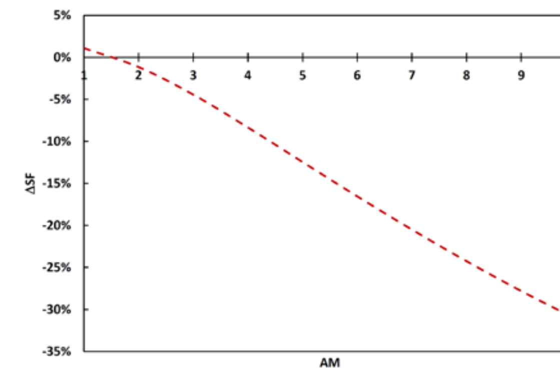

Fig.3. Effect of air mass on the perovskite solar cells performance. The other parameters are kept constant at the reference values defined by the AM1.5G ASTMG-173-03 reference spectrum.

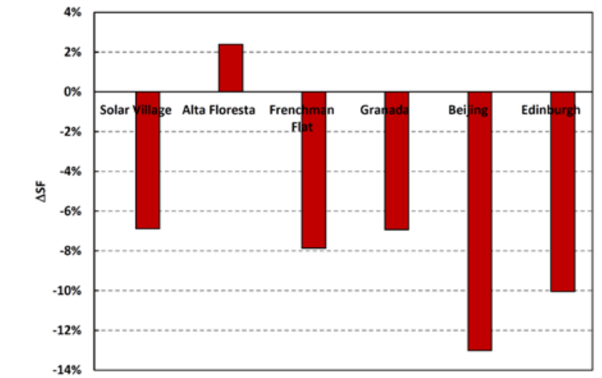

Fig.4. Annual impacts of the spectral variations on the performance of perovskite solar cells at the six different locations.

Location	AM	$\tau_{0.55}$	α	w
Solar Village	4.0	0.35	0.56	1.23
Alta Floresta	3.1	0.31	1.27	3.92
Frenchman Flat	5.0	0.07	1.15	0.89
Granada	5.0	0.15	1.07	1.27
Beijing	5.3	0.74	1.08	1.28
Edinburgh	7.5	0.09	1.00	1.14

Table 1. Annually-average values of air mass (AM), aerosol optical depth at 555nm ($\tau_{0.55}$), Ångström exponent (α) and precipitable water (w).

Short Channel Effects in Graphene Field-Effect Transistors

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1. Introduction

Graphene has attracted much attention in the world of high-frequency electronics because of its high carrier mobility and saturation velocity [1]. An excellent cutoff frequency f_T of 427 GHz has been reported for a graphene channel field effect transistor (GFET) with a channel length of 67 nm [2] and the theoretical limit has been predicted to be over 1 THz, well above all other high-frequency technologies [3]. However, to reach higher f_T (related to current gain) and maximum frequencies of oscillation f_{max} (power gain) the use of transistors with lower dimensions is necessary. Although this two dimensional material should, in principle, provide more immunity to short channel effects (SCE) than bulk materials due to the improved gate control over channel potential, that has not been demonstrated yet. Thus, the study of GFETs with very small dimensions, where SCE could certainly play an important role, becomes mandatory in order to determine the limits of aggressive scaling.

2. Short channel effects

In Ref. 4, Shu-Jen Han *et al.* present a systematic experimental study of SCE in GFETs. In that work, they conclude that SCE influence noticeably the Dirac voltage (V_D) shift upon application of a source-drain bias (V_{ds}). Figure 1 compares this shift for long channel and a short channel situation. Short channel lengths shift V_D in opposite direction upon application of a drain bias as compared with long-channel devices. They also find an asymmetry between the electron and the hole branches of the transfer characteristics (drain current I_{ds} vs. gate voltage V_{gs}). They associate it with contact effects, which may be more noticeable in short channel devices.

Our work consists in developing a physics-based model to study SCE via the solution of the two-dimensional Poisson equation. Figure 2 shows the electrostatic potential coming from the solution of Poisson equation for a dual gated GFET consisting of 40 nm Al_2O_3 as top gate dielectric (relative permittivity $\epsilon_r = 21$) and 400 nm SiO_2 as bottom dielectric ($\epsilon_r = 4$). The graphene layer lies along $y = 0$. Figure 2 (a) corresponds to a channel length L of 10 µm while in figure 2 (b), $L = 50$ nm. Charge-neutrality top gate voltage V_{gs0} has been considered as 0.85 V in both devices and the bias cconditions are $V_{ds} = 0.8$ V, $V_{gs} = 1.25$ V and back gate voltage $V_{bs} = 0$ (charge neutrality back gate voltage $V_{bs0} = 0$). From this model, I_{ds} can be calculated taking into account SCE. Figure 3 shows that the electrostatic potential drop along the channel seems to be concentrated around source ($x = 0$) and drain ($x = L$) for the short channel transistor while this drop is softer along the position x for the long channel transistor.

3. Conclusions

In this work we deal with the electrical modeling of GFETs with small dimensions via the solution of the two-dimensional Poisson equation and further calculation of the drain current using a drift-diffusion transport equation. The goal is to understand the consequences of SCE in GFETs, taking as a reference some reported experimental results.

4. Acknowledgements

The research leading to these results has received funding from Ministerio de Economía y Competitividad of Spain under the project TEC2012-31330 and from the European Union Seventh Framework Programme under grant agreement n°604391 Graphene Flagship.

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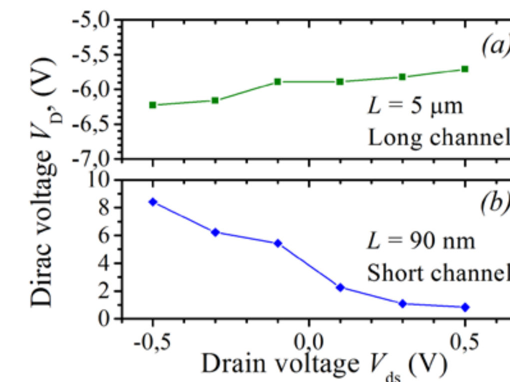

Figure 1. Dirac Voltage shift with source-drain voltage for a long channel device (a) and a short channel device (b). Data taken from ref. 4.

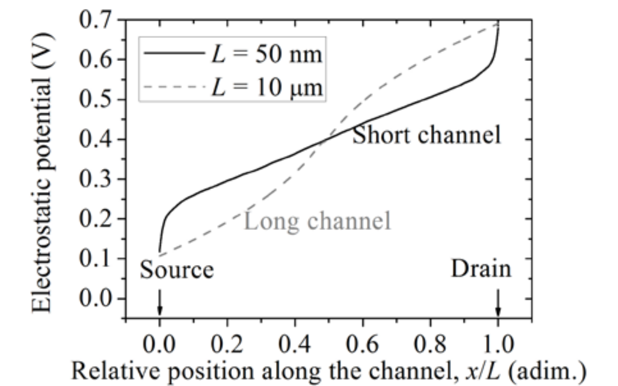

Figure 3. Electrostatic potential as a function of the position within the channel for a short channel and a long channel device.

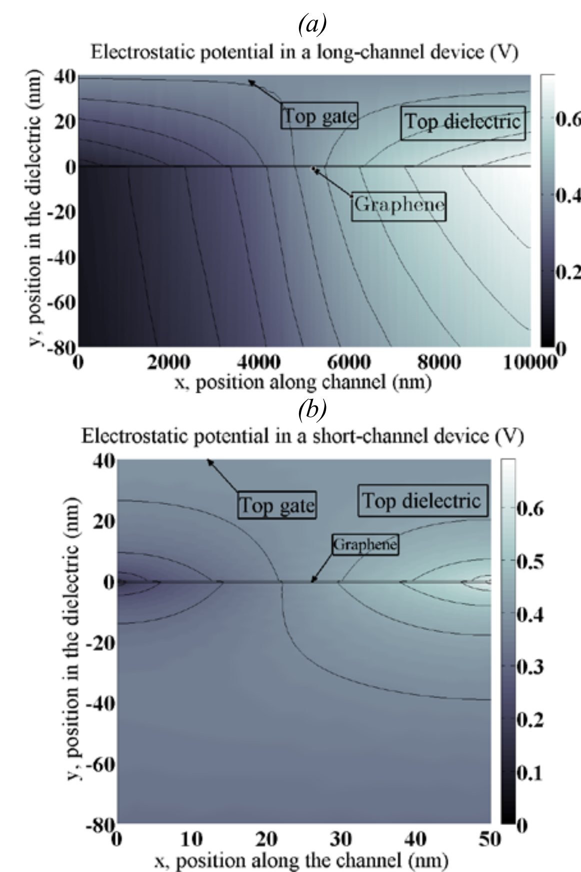

Figure 2. Electrostatic potential of a prototype GFET, considering long-channel (a) and short-channel (b) devices.

Impact of millisecond anneal induced for ultra-shallow junctions on Negative Bias Temperature Instability

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1. Abstract

In this paper the NBTI degradation has been studied in pMOS transistors with ultra-thin high-k dielectric subjected to a millisecond anneal for ultra-shallow junction implantation using different laser powers. An ultrafast characterization technique has been developed with the aim of acquiring the threshold voltage (V_{th}) shift in relaxation times as short as possible once the electrical stress is removed. It has been observed that increasing the millisecond anneal temperature reduce the NBTI degradation. These results have been explained in the context of the emission and capture probability maps of the defects.

2. Introduction

Ultra shallow junction formation in deeply scaled CMOS technologies requires the optimization and control of the implanted dopants. To achieve this objective millisecond anneal (MSA) has been shown to be a promising technique for the 32nm node and below [1]. On the other hand, Negative Bias Temperature Instability (NBTI), one of the main aging mechanisms in CMOS devices, is strongly dependent of the fabrication process [2]. Although some prior work has been done about the influence of MSA on NBTI degradation [3], here we will extend these studies from very short to medium relaxation times. Moreover, the results will be interpreted in the framework of the recent advances in the NBTI physics modeling.

3. Experimental

The samples were pMOS transistors with $HfSiO/Al_2O_3$ as dielectric stack, TaCN as gate electrode and W/L=10µm/0.15µm. The MSA was applied for the activation of the source/drain implantations by means of a laser pulse on transistors; low (LLP), medium (MLP) and high (HLP) laser powers were studied. The temperatures achieved during the three types of annealing are estimated to be 1100ºC, 1200ºC and 1350ºC; the duration of each anneal is around 1 ms. To provoke the NBTI degradation, constant voltage stresses (CVS) of 10s, 100s and 200s were applied. After each CVS the devices were relaxed during 150s. The threshold voltage was measured during the relaxation using an ultra-fast (UF) set up [4] (Fig. 1). The system operates at two modes, measure or stress, which can be interchanged by means of three digital switches. At the stress mode, a CVS is applied to the device; at the measure mode, 100mV were applied to the drain and the source was grounded. In this mode a current through the channel is forced by means of I_{bias}. If the value of I_{bias} is properly chosen, the transistor operates at $V_G=V_{th}$. Finally V_{th} evolution during relaxation is measured using an oscilloscope. With this setup values of V_{th} can be obtained after 20us of relaxation. Note that the negative feedback of the amplifier is maintained when the modes are interchanged, avoiding voltage ripples that could be detrimental for the measurement.

4. Results.

Fig. 2 shows the fresh (non-stressed) I_d-V_G characteristics in linear and semilog scale. Clearly, a high V_{th} shift reduction is observed for MLP and HLP conditions [1]. In Fig. 3 the BTI relaxation traces after the CVSs are plotted. Increasing the laser power significantly reduces the NBTI degradation, which could be related to an annihilation of defects at high temperatures during the MSA. To model the V_{th} traces in Fig. 3, the occupancy maps (that is, the probability that a defect with given emission and capture times is occupied) at the measurement conditions have been calculated [4,5]. The defects were considered to follow a bivariate distribution in the log (τ_e)-log(τ_c) map (a second bivariate distribution should be considered for long stress and relaxation times or extrapolations) [6]. Fig. 4 shows the distribution obtained for samples with LLP, MLP and HLP. Note that similar distributions are obtained for the three types of samples; however the k parameter (related to the number of active defects) decreases with the laser power. Finally, the V_{th} shift obtained at different stress voltages can be fitted by an exponential law (Fig. 5). A very similar exponent (α) is obtained for devices with different laser power anneal, which supports the hypothesis of defect passivation by the annealing.

5. Conclusions

NBTI degradation in pMOS transistors with high-k dielectric has been studied when a millisecond anneal is used for ultra-shallow junction implantation using different laser powers. The results show that V_{th} degradation caused by NBTI can be correctly described using the occupancy maps of defects within the device. Moreover, the defect distribution in the emission-capture times space can be obtained. The laser power significantly reduces the BTI degradation, improving the device reliability. This effect has been associated to the defect passivation during the device annealing.

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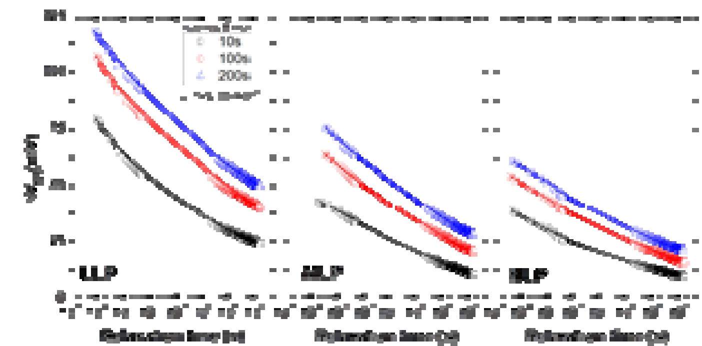

Fig. 3 V_{th} shift as a function of relaxation time obtained after stresses at -2.1V. Increasing the power of the laser anneal significantly reduce the NBTI degradation.

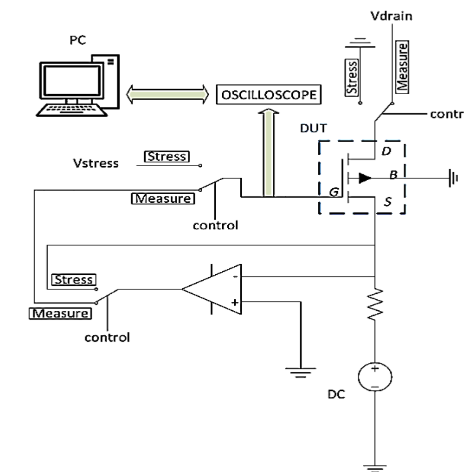

Fig. 1 Schematic setup used to perform ultrafast measurements.

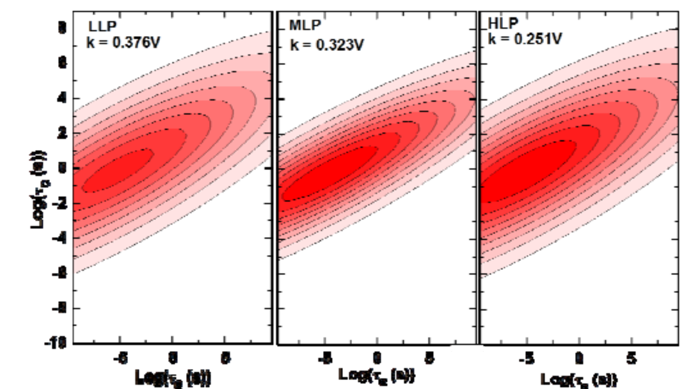

Fig. 4. Defect distribution in the τ_c-τ_e space. Similar distributions are obtained for the three laser powers considered. The k parameter (related to the number of defects in the device) decreases with the laser power.

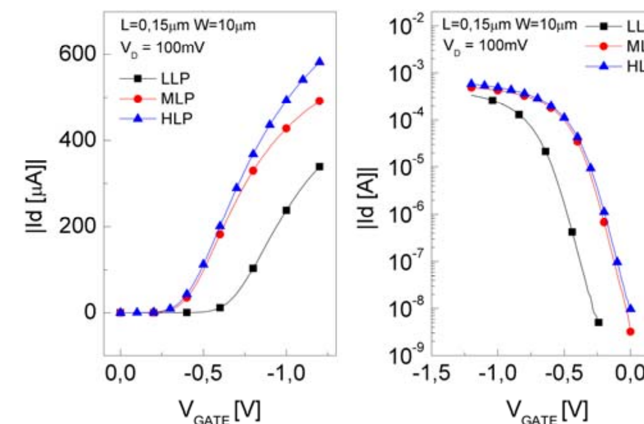

Fig. 2 Id-V_G characteristic in linear (left) and semilog (right) scale of fresh devices. Transistors with LLP show a higher threshold voltage.

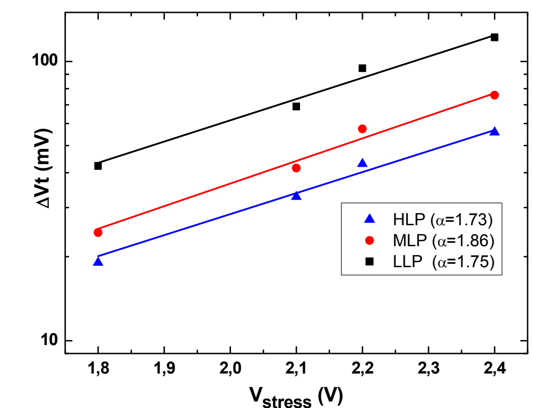

Fig. 5. V_{th} shift as a function of stress voltage for different powers of the laser anneal. The V_{th} shift values where obtained after 10s of stress and 0.3s of relaxation.

Compact Device for CO_2 Optical Sensing using Macroporous Silicon Photonic Crystals

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1. Abstract

A photonic crystal based on a macroporous silicon structure has been fabricated and successfully used for the detection of carbon dioxide. In this paper, the device and the measurement results are presented. The sensing device here described uses an optical approach to the detection of the gas. The use of a photonic crystal allows creating a compact device working in the medium infrared spectral range. A 700 nm square lattice macroporous structure was fabricated by electrochemical etching, creating a photonic gap centred at the 4.2 µm, a CO_2 absorption line. The obtained results rely only on the absorption spectra measurement.

2. Introduction

Gas sensing, detection and quantification can be done employing a broad variety of techniques [1]. Commercial sensing devices, depending on their application, have several requirements in size, portability, sensitivity and selectivity. Commonly found for commercial applications are sensors based on metallic oxides or polymers. Though these type of sensors fulfil the first two premises, there are somewhat lacking in others such as selectivity or response times. Furthermore, some kinds of sensors can have high power demand, and may suffer degradation, either from aging, or contamination. On the other hand, optical sensing devices usually have good sensitivity and excellent selectivity and have fast responses, but often are laboratory grade equipment. Recently, compact devices based on the measurement of an optical response have been described [2]; other works [3] propose the use of macroporous silicon for gas sensing.

3. Fabrication and Measurement

Macroporous silicon structures used in this work were fabricated using the light assisted electrochemical etching technique (EE) for silicon described in [4]. N-type wafers were etched in a hydrofluoric acid bath controlling the pore profile by light modulation. The fabricated structures are square lattices of ordered pores with a 700 nm pitch and pore diameter around 500 nm with a soft modulation, as seen in **Fig. 1**. The structures where characterized by FTIR reflectance measurement in the MIR range from 2 µm to 20 µm. A reflection peak can be observed (**Fig. 2**) in the 4.2 µm CO_2 absorption line. Afterwards the sample was placed in an enclosed cell through which CO_2 at different concentrations flowed. Reflectance was measured at normal incidence through a potassium bromide window at a 0.5 mm gap from the sample.

4. Results and Discussion

The fabricated macroporous structure as shown in **Fig. 2** has a 30% reflectance peak at the CO_2 absorption line. Though this peak is good enough, better values should be possible. As the SEM image in **Fig. 1** reveals, this is due to the soft modulation and structure irregularities. Work is being done to improve the reflection peak, improving the reflectance, and it also should increase sensitivity. From the reflectance measurements, absorption spectra for CO_2 concentrations from 5% to 50% was extracted, as shown in **Fig. 3**. From the obtained results a clear variation of absorbance can be observed for different gas concentrations.

5. Conclusion

Gas sensing compact devices based on a macroporous silicon photonic crystals have been successfully fabricated with a photonic bandgap at the 4.2 µm absorption line of CO_2. They were tested for several gas concentrations and the absorbance spectra obtained shows a clear relationship with concentration.

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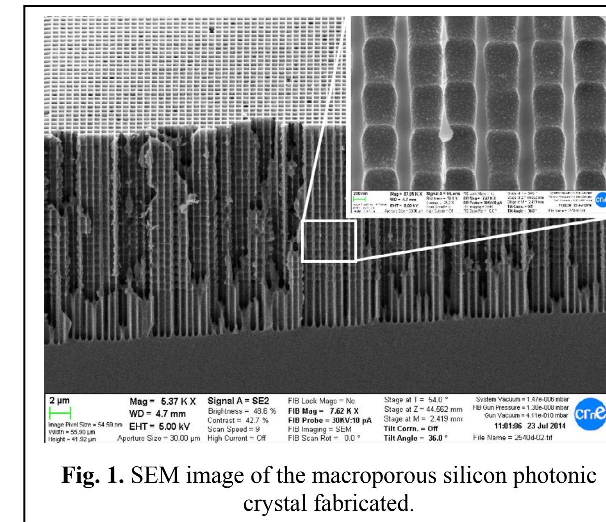

Fig. 1. SEM image of the macroporous silicon photonic crystal fabricated.

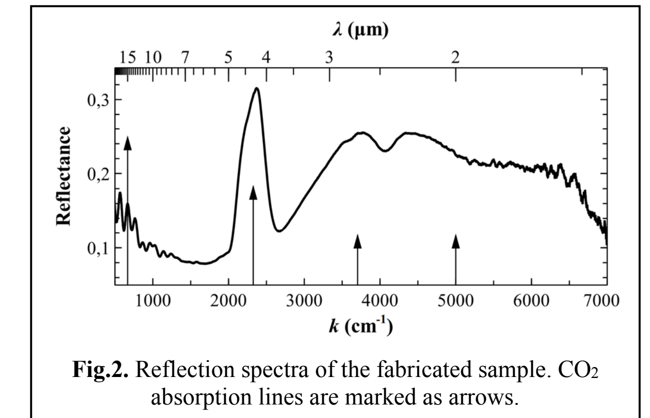

Fig.2. Reflection spectra of the fabricated sample. CO_2 absorption lines are marked as arrows.

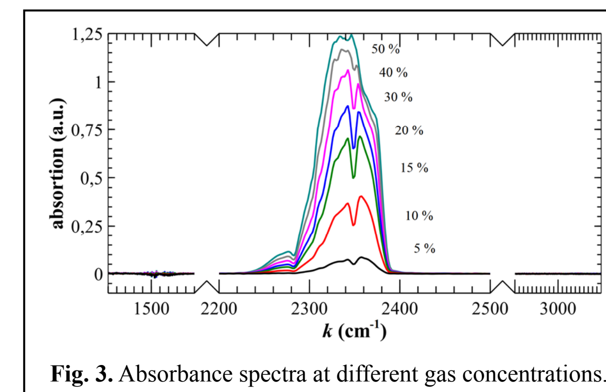

Fig. 3. Absorbance spectra at different gas concentrations.

Simulation of the phonon-limited electron mobility in multi-layer MoS_2 field-effect transistors

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1. Abstract

We study the electron mobility in Metal-Insulator-Semiconductor Field-Effect-Transistors which use multi-layer MoS_2 as channel. The electrostatic behavior is calculated by self-consistently solving the 1D Poisson and Schrödinger equations under the effective mass approximation. Phonon-limited electron mobility is then calculated solving the Boltzmann Transport Equation under the Momentum Relaxation Time approximation for different device sizes and bias conditions.

2. Introduction

The use of 2D materials as an alternative to traditional Si-based technology has driven the attention of the scientific community during the last years. Following the trail of grapheme, transition metal dichalcogenides, and in particular MoS_2, provide interesting properties, including the capability of ultra-thin (up to atomic layer thin) body devices. Some works deal with the modeling of monolayer MoS_2 phonon-limited mobility [1]. However, its behavior for multilayer MoS_2 devices is not so well explored. Kim et al. [2] have examined the mobility of thick MoS_2 FET structures employing bulk expressions for the electron mobility, but such an approach is not accurate for thin inversion layer devices. We analyze here the phonon-limited electron mobility (μ) of MoS_2 FETs considering the confinement quantization, in an approach that can be useful for multilayer MoS_2 devices down to a few atomic layers.

3. Numerical model

The cross-section of the simulated device is depicted in Fig. 1. Wide and long-channel devices are assumed, being therefore their electrostatic behavior properly described using a 1D self-consistent Poisson-Schrödinger solution. The Effective Mass Approximation (EMA) is employed as it has been reported that, for more than 6 atomic layers, the MoS_2 band structure resembles that of bulk MoS_2 [3]. The conduction band is characterized by six equivalent valleys, distributed along the Γ-K symmetry lines (Λ points, see Fig. 1), which are here modeled using an isotropic density-of-states effective mass, different from the confinement effective mass. The values employed are extracted from [4] and summarized in Table 1. As for μ calculation, we include transversal and longitudinal acoustic phonons (TA and LA), longitudinal optical phonons (LO), homopolar phonons (HO) and polar optical phonons due to Frölich interaction (POP). The parameters employed (Table 2) are extracted from [1], where they are calculated for monolayer MoS_2. The expressions used to model the different phonon scattering probabilities in inversion layers can be found in [5]. Once the scattering rate of each mechanism is calculated, the Momentum Relaxation Time approach is used to solve the linearized Boltzmann Transport Equation.

4. Results

We have first calculated the scattering rate due to each scattering mechanism for two devices with thickness T_{sc}=10nm and T_{sc}=2nm, respectively (Fig. 2). As can be seen, POP is the main scattering mechanism. This conclusion is consistent with the results presented by Kim et al. for thick devices in [2]. On the other hand, homopolar phonons do not seem to play a very relevant role regardless of the device size. For the smaller device, the influence of acoustic phonons is more noticeable, in particular in the region close to E_c=0. Again, this behavior is consistent with the conclusions achieved in [1] for monolayer MoS_2 FETs. Then, we have analyzed the behavior of μ for devices with three different T_{sc} values (2nm, 5nm and 10nm) as a function of the inversion charge (N_i). As shown in Fig. 3, μ remains almost constant in the whole N_i range for the three different semiconductor thicknesses. There is however a strong influence of the MoS_2 thickness on the electron mobility, as a non-monotonic tendency is found. This behavior is analyzed in detail in Fig. 4, where μ is depicted as a function of T_{sc} for N_i=5x10^{12}cm^{-2}, and a maximum is observed around T_{sc}=5nm. The mobility associated to each scattering mechanism has also been plotted, showing that POP and LO phonons cause the non-monotonic mobility trend, while acoustic phonons monotonically grow with T_{sc}.

5. Conclusion

This work presents a simulation study of the electron mobility in FETs with a multi-layer MoS_2 channel. The electrostatic behavior is described through the self-consistently solution of the 1D Schrödinger and Poisson equations, under the EMA. The results obtained for the phonon-limited electron mobility depicts an almost independent behavior with the charge density and a non-monotonic behavior with the MoS_2 thickness, having a maximum around 5nm of MoS_2 thickness and decreasing for thinner devices. We would like to highlight that these results are for phonon-limited mobility only, and a different behavior could be found if other scattering mechanisms were considered.

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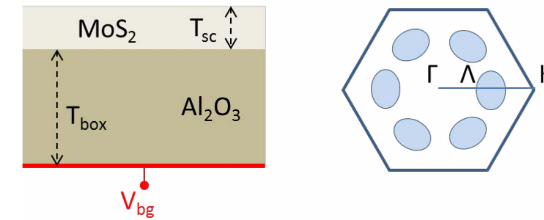

Fig.1. Geometry of the back-gate MoS_2 FET device (left) and schematic representation of the six degenerated Λ valleys (right).

MoS_2	
Dielectric constant	ε_r=7
Λ valleys degeneration	d_v=6
Confinement effective mass	m*=0.49m_0
Density-of-states effective mass	m_{DOS}=0.62m_0
Al_2O_3	
Dielectric constant	ε_r=9
Potential barrier	ΔE_c=2.6eV
Effective mass	m*=0.2 m_0

Table 1. Simulation parameters for electrostatic calculation. Extracted from [2,4].

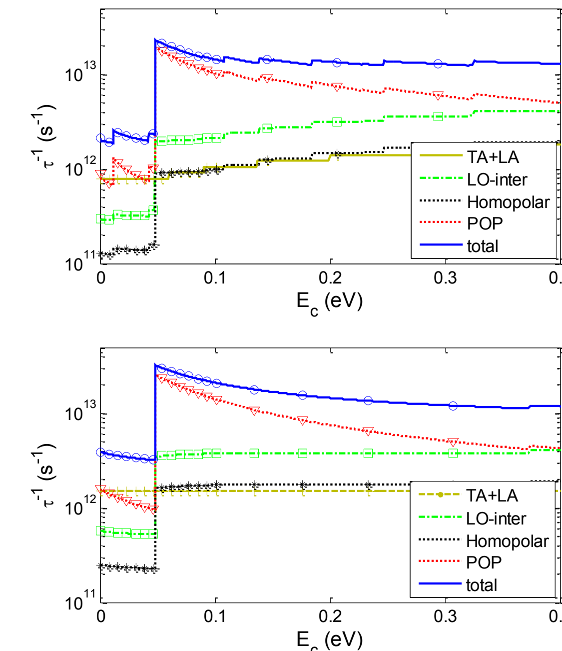

Fig.2. Inverse momentum relaxation time of the first subband as a function of E_c, for T_{sc}=10nm (top) and 2nm (bottom), and N_i=5x10^{12}cm^{-2}. The contribution of each scattering mechanism is also depicted.

Acknowledgement
Work supported by the Spanish Government under the project FIS2011-26005. J. M. González-Medina and E.G. Marin also acknowledge the *Plan Propio de Investigación* of the University of Granada.

Parameter	Value
MoS_2 density	ρ=7.03x10^{-3} kg/cm^3
LA deformation potential	D_{LA}=2.8eV
Longit. sound velocity	v_l=6.7x10^5 cm/s
TA deformation potential	D_{TA}=1.6eV
Transversal sound velocity	v_t=6.7x10^5 cm/s
HO deformation potential	D_{HO}=4.1x10^8 eV/cm
HO phonon energy	E_{HO}=50 meV
LO deformation potential	D_{LO}=2.6x10^8 eV/cm
LO phonon energy	E_{LO}=48 meV
LO intervalley degeneration	d_v=5
POP phonon energy	E_{POP}=48 meV
HF dielectric constant	ε_∞=7ε_0

Table 2. Scattering parameters employed for mobility calculation (after [1]).

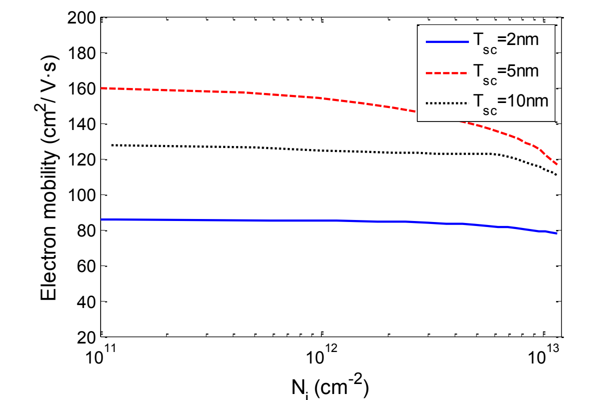

Fig.3. Phonon-limited electron mobility as a function of the inversion charge, for device thickness T_{sc}=2nm (solid), 5nm (dashed) and 10nm (dotted).

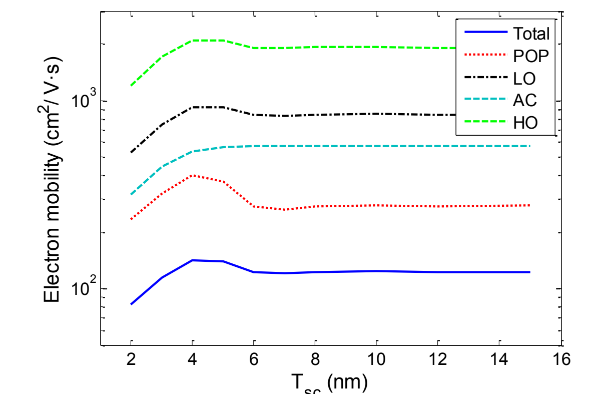

Fig.4. Phonon-limited electron mobility as a function of the device thickness, for N_i=5x10^{12} cm^{-2}. The mobility associated to each scattering mechanism is also shown.

Calculation of self-heating in cryogenic InP HEMTs by Monte Carlo simulations of phonon and electron transport

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1. Introduction

Heat dissipation in transistors occurs in a two-step process in which electrons in the transistor channel emit phonons that then carry the heat away from the active region [1]. The processes that impede phonon transport in these devices are thus of critical importance as they determine the self-heating that occurs in the device. Here, we investigate thermal dissipation mechanisms in cryogenic InP HEMTs using Monte Carlo simulations of electron and phonon transport. We show that heat dissipation at cryogenic temperatures in these devices occurs by phonon blackbody radiation that results in large self-heating in the limit of zero ambient temperature. Our work demonstrates that this fundamental limit on heat dissipation is a key consideration in the performance of ultralow noise electronic devices.

2. Simulations of electron transport

The electron transport and the consequent phonon emissions have been simulated using a 2D semiclassical Monte Carlo model for electron transport (MCE). This model correctly reproduces the DC, AC and noise behaviour of InP HEMTs both at 300 K [2] and at cryogenic temperatures [3]. We obtain the spatial distribution of dissipated power and hence phonon generation for the phonon BTE simulations by recording the energy balance of the electrons at each mesh point over 0.1 ns. Fig. 1 shows the distribution of power associated with phonon emissions in the HEMT of [3] obtained with the MCE simulator when biased at low noise bias conditions (V_{ds}=0.5 V and I_d=20 mA/mm) at 77K. We find that most of the phonon emissions take place in the channel at the drain edge of the recess. We performed the electrical simulations at temperatures ranging from 300 K downto 30 K. We find the distribution of phonon generation to be constant in the low temperature range below 150 K where electron transport is completely ballistic under the gate, so that a self-consistent approach with the phonon transport simulations is not necessary under cryogenic conditions.

3. Simulations of phonon transport

Instead of solving the heat diffusion equation using the thermal conductivities of the different materials that make up the transistor, we solve the phonon Bolzman transport equation (PBTE) using variance-reduced Monte Carlo algorithms that simulate the advection and scattering of computational particles (representing phonons) in a 2D domain [4]. In these algorithms a computational particle represents a fixed amount of deviational energy from an equilibrium Bose-Einstein distribution rather than a constant number of phonons as in previous algorithms. The algorithm directly solves for the steady-state solution of the PBTE by sequentially advecting and scattering the phonons in the domain. The temperature and heat flux from the phonons is obtained by spatially discretizing the domain and recording the time spent and the velocity of each phonon in a particular cell. On top of the device, we enforce an adiabatic condition in which phonons are reflected back with equal probability in the hemisphere defined by the boundary normal because the gate and passivation layer are isothermal with the top of the device layer. The InP substrate is treated as semi-infinite with phonons that have traveled sufficiently far away from the channel being deleted. The heat generation in the channel is incorporated as a volumetric heat generation process. Phonons are generated in a specified location and volume determined from the previously described MCE simulations with random velocity directions on a unit sphere and an equilibrium distribution in frequency. See more details in [5].

The steady state temperature profile of the transistor with this heating distribution at different ambient temperatures for the same input power used in the measurements is shown in Fig. 2. At 300 K, Fig. 2(a), the temperature in the channel is nearly the same as the ambient. The phonon mean free path increase rapidly with decreasing temperature, and temperature rise in the channel is still minimal at 20 K, Fig. 2(b). Below 20 K the peak temperature in the channel remains nearly constant despite the substantial decrease in ambient temperature. These results is consistent with noise measurements made in cryogenic amplifiers made with InP HEMTs and allow us to explain the self-heating as a consequence of heat conduction by phonon blackbody radiation (instead of the classic heat dissipation based on the diffusion theory) [5].

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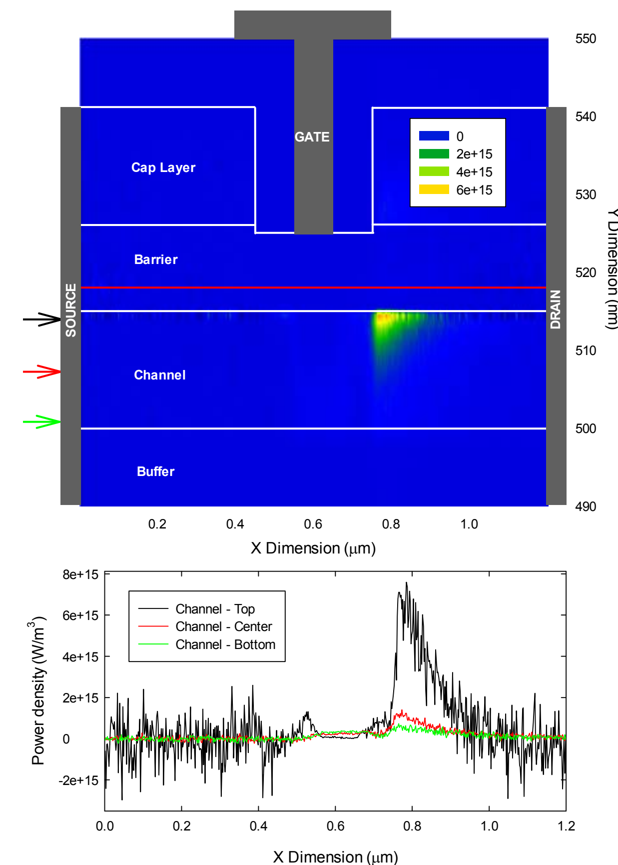

Fig. 1. Distribution of emitted power associated to phonon emissions obtained with Monte Carlo simulations of electron transport at 77 K. V_{ds}=0.5 V and I_d=20 mA/mm.

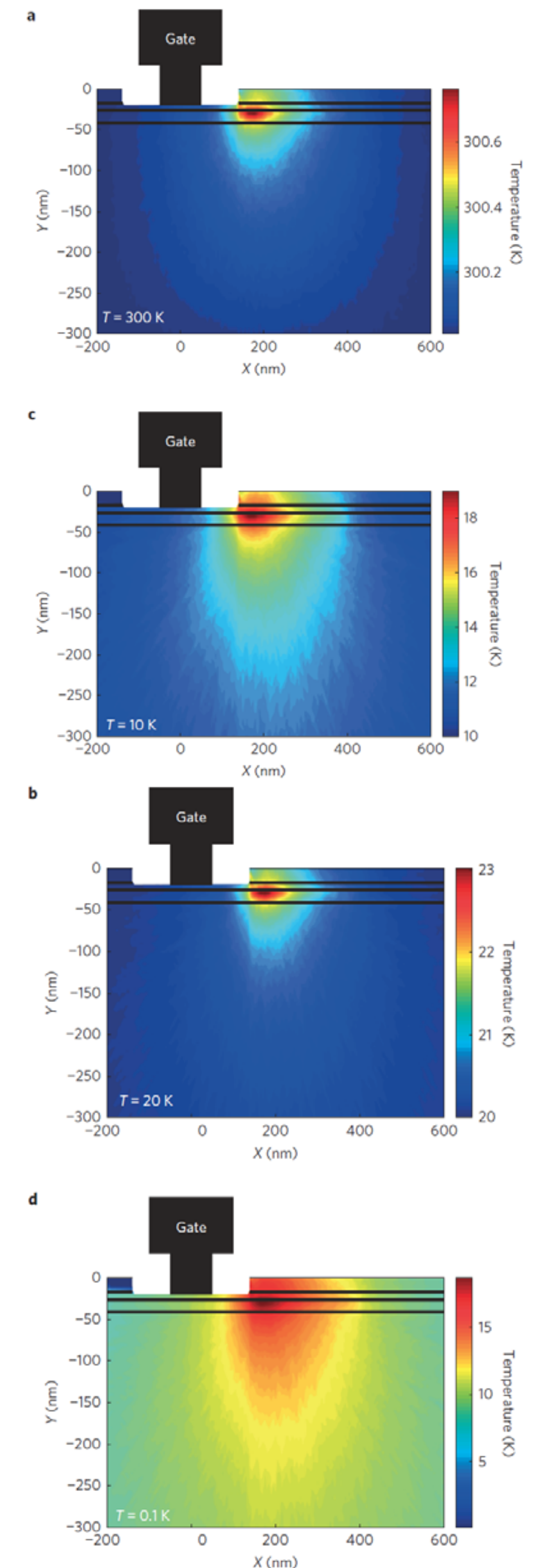

Fig. 2. Steady-state lattice temperature profiles with 29 mW/mm input power for ambient temperature of (a) 300 K, (b) 20 K, (c) 10 K, (d) 0.1 K.

Impact of the Absorption in Transmittance and Reflectance on Macroporous Silicon Photonic Crystals

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1. Abstract

Photonic Crystals (PC) were introduced almost simultaneously in 1987 by Eli Yablonovitch [1] and Saajeev John [2]. They showed that propagation of certain wavelengths could be inhibited in a Photonic Crystal. Since then, a wide variety of applications have been proposed, in particular, gas detection is of great interest. By introducing a defect in the PC, a reflection dip or a transmission peak can be accurately placed in a desired wavelength, corresponding to an absorption line of the gas to be detected. In addition, irregularities and losses play a key role in PC-based optical applications. In this paper we report the influence of the material losses in the reflection or transmission peaks in order to estimate its maximum acceptable value for gas sensing applications and their effect in the response of the sensors.

2. Motivation of the study

Photonic Crystals allow the inhibition of light propagation at certain frequencies and directions. By modifying its regular structure, i.e. introducing a defect inside it, light can propagate through the crystal in the forbidden band. This phenomenon can be used for gas detection. The basic sensing setup is composed by an emitter [3], a receiver and a volume in where light interacts with the gas to analyze. Within the bandgap, the reflectance of a Photonic Crystal is very high except for the defect wavelength, where there appears a dip in the reflection spectra. In the same way Photonic Crystals can be designed to exhibit a peak in reflection around a given frequency. These peaks and dips will be tuned to a particular wavelength where the target gas has a distinctive absorption feature and, therefore, by analyzing the signal in the receptor, the presence and concentration of the gas can be determined.

The application of Photonic Crystals for gas sensing, allows the fabrication of devices with very fast response times and a high specificity which, added to the low cost of their production, make them good candidates to compete with commercial gas sensors.

The most important element in the gas sensor described above is the Photonic Crystal. Its optical properties will depend on both the periodicity of the structure, and the material's optical properties. These are described by its refractive index which, in general, is a complex number $\hat{n} = n + j \cdot k$. The imaginary part k, called extinction coefficient, is related to the dielectric absorption losses. The higher the imaginary part, the higher the absorption losses and the lower the Q-factor of the transmitted peak. In fact, the study of perfect Photonic Crystals implies the absence of losses. Real materials, however, present optical losses that will influence the actual characteristics of the sensors. In this work, the impact of the material losses in the reflection/transmission peaks are studied, and their influence is evaluated. The goal of this work is to elucidate guidelines to determine the upper boundary of optical losses that can be tolerated for a correct operation of the devices.

3. Simulation and conclusions

Electromagnetic propagation in the considered Photonic Crystals has been simulated by the FDTD technique using Optiwave's OptiFDTD software package. The photonic structures consist of an array of pores inside a silicon wafer. This structure is an approximation of the ones we can fabricate in our laboratory (see Fig.1). In this work the dependence of the characteristics of the reflection peaks are studied. .

In Fig. 2 we observe that the decline of the band reflectance respect to the absorption depends as an exponential function. Results of this work also show that the width of the transmission peak remains fairly constant while the height of the peak decreases, as losses increase.

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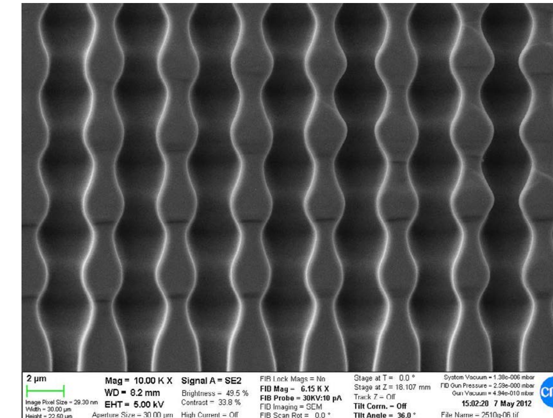

Fig.1. Profiles made by MNT group for gas sensors applications.

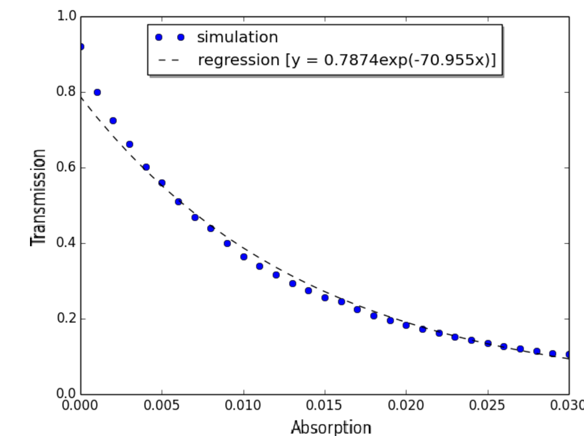

Fig.2. Response of the transmission amplitude depending on the silicon absorption.

Influence of Doping on the Optical Response of GaInP

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1. Introduction

The precise determination of the physical parameters of ternary alloys has been the goal of many studies during the last decades [1]. The respective binary alloys are often used as a reference in order to deduce or interpolate the desired parameter; however, in many cases the results of this method differ from the experimental results. For the case of the band-gap, there are several known factors such as temperature or doping which could produce band energy shifts [2-4]. The band-gap is usually determined by photoluminescence, nevertheless it is an optical technique, it does not allow a complete characterization of the optical response of a material. In this work Variable Angle Spectroscopic Ellipsometry (VASE) has been used to determine the refractive index and extinction coefficient of doped and undoped samples of GaInP, allowing a simultaneous deduction of the band-gap.

2. Experimental

Three GaInP samples with different Zn doping levels were epitaxially grown on (100) GaAs wafers misoriented 2º towards the nearest (111)A plane in a low pressure horizontal Aixtron MOVPE (AIX-200/4) reactor. Trimethylgallium (TMGa), trimethylindium (TMI) and phosphine (PH_3) were the sources used for the GaInP layer. DMZn was used as the doping source. The doping concentration of the samples was measured by capacitance-voltage (CV), the results are shown in table 1. The samples have been characterized by a spectroscopic ellipsometry analysis in variable angle mode in the range of 1.3 to 5 eV at room temperature, followed by scanning electron images on the cross sections of the samples.

The model fitting and regressions of the ellipsometric analyses have been carried out using SEA 1.3 from SEMILAB. The chosen model to describe the optical properties of GaInP consisted of two Tauc-Lorentz oscillators and one Adachi 3D term for energies higher and around the band-gap, and a Cauchy term describing the samples for energies lower than the band-gap.

3. Results and Discussion

The images of the cross sections of the GaInP samples (see Figure 1) have allowed to measure thickness of the sample layers, later it has been used as input data for the ellipsometric analyses. There is a very high agreement among the SEM measurements and the results of the fitting process of the ellipsometric measurements as can be seen in table 1.

The model used describes satisfactorily the samples in the analyzed photon energy region as can be seen in Figure 2, with coefficients of determination (R^2) over 0.99, allowing to deduce the optical behavior. In figure 3 it is possible to see the extinction coefficient for the different samples (top); in the vicinity of the band gap (bottom). When approaching the zero point in the extinction coefficient, the band-gap values have been deduced by a graphical method. The band-gap increase observed when Zn dopant amount does, may be related with the microscopic disorder induced by Zn doping at high enough concentrations [5].

Spectroscopic elipsometry is thus a non-destructive technique which allows the complete characterisation of the material optical response, extending the provided information to the whole spectral range. This method is particularly interesting for the design of optoelectronic devices such as optic sensors or solar cells [6, 7].

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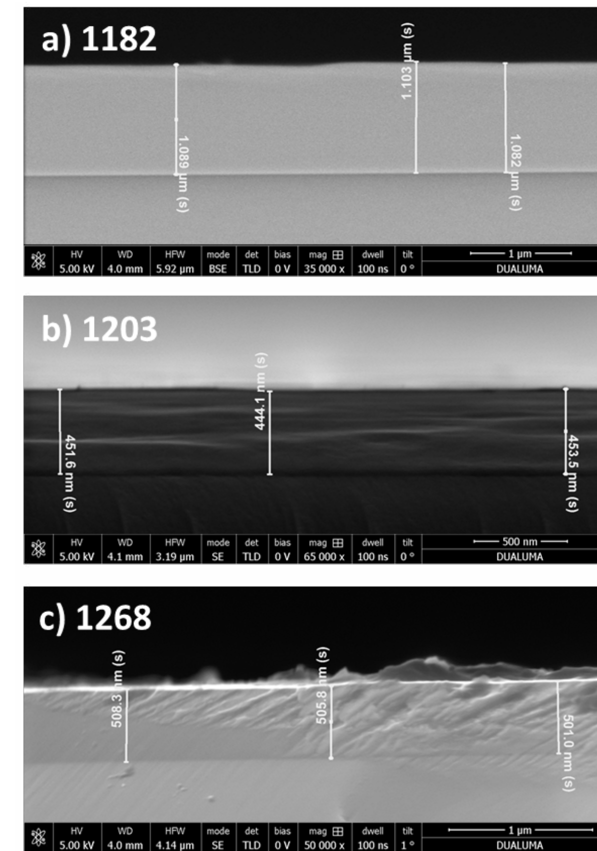

Figure 1. SEM images of the cross section of GaInP samples.

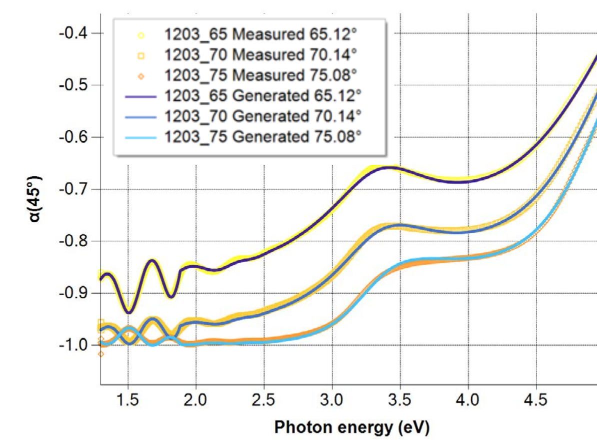

Figure 2. 1203 sample VASE acquisition and model fit.

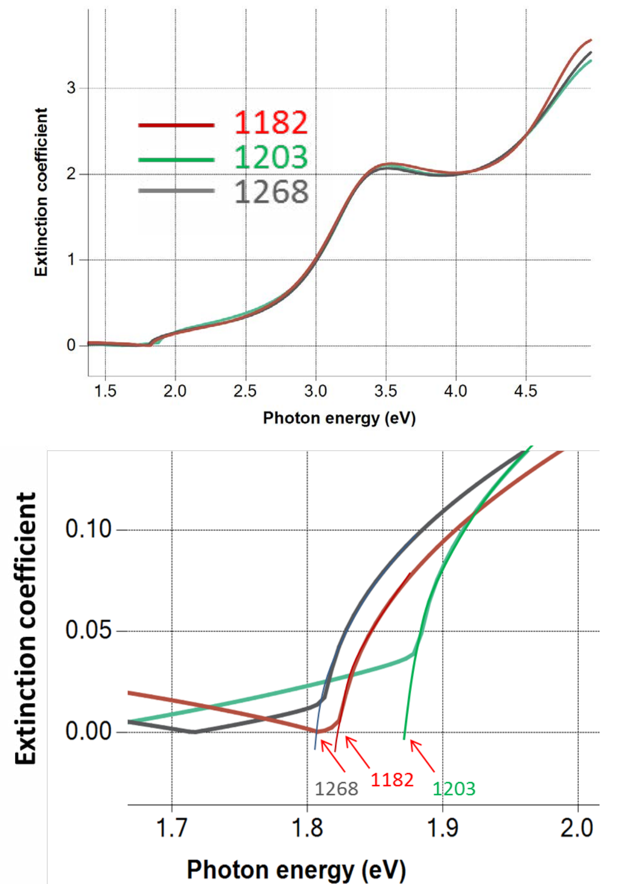

Figure 3. Extinction coefficient for GaInP samples (top) with detail of the bandgap vicinity (bottom).

Sample	Band-gap (eV)	Doping level	Thickness (nm)	
			SEM-Fib	Ellipsometry
1182	1.822	3.1E16	1093.2 ± 7.1	1072
1203	1.871	1.58E17	454.5 ± 8	451
1268	1.806	Undoped	502.7 ± 4.5	511

Table 1. Sample physical properties.

Comparison of state-of-the-art distributed computing frameworks with the GWM

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1. Abstract

We analyze the landscape of computing solutions available to deploy scientific workloads in heterogeneous computing resources. We aim to compare the existing solutions with our provided application, the General Workload Manager, to offer a full and rich explanation of the state of the art in production environments for the management of computational workloads. We have successfully found several similarities, and also key differences with our provided software, and stablished a comprehensive explanation of the computing landscape.

2. General Workload Manager

We have developed a general purpose application capable of deploying computational workloads, like those needed to undertake nanodevice simulations, in heterogeneous computing resources. This application, see Fig. 1, is not tailored to any single application, does not require any instalation or configuration in the target machines that will deploy the tasks, and is meant to be used for computational workloads like simulations, data transformation, analysis, or any other task that require a set of input data, a time-bounded task and the retrieval of the result from the task execution. The system run in local (Fig. 2) and server (Fig. 3) operation mode.

3. GRID applications

Several solution have been developed over the existing Grid infrastructure. These solutions are defined similarly to an application layer. This layer consists on providing a set of tools and interfaces, such that an inexperienced user in the field of Grid computing is able to harness the computational resources provided by the infrastructure. These applications, nonetheless, are only tailored to certain fields, in order to provide easy to use and tightly binded interfaces. So, as a downside of having very well tailored interfaces, easy to use tools, and a high integration with the workflow and dataflow of the scientific field being deployed into the system, the field of application for each of this applications is narrow. Each application has only capabilities to fullfill a narrow scope, and so several solutions has to arise in order to deal with the heterogeneous computing neccesities. In contrast, our GWM is capable of deploying several different workloads, without any bound to the underlying problem. Some visualization capabilities and tools can be easily designed over the infrastructure defined by the GWM. Examples: GridF, Retelab, The Earth System Grid

4. Middleware

Another set of similar software present in the computing landscape is the middleware applications for Grid computing. These middleware are an heterogeneous set of very big and difficult to mantain software packages that interact closely with the underlying Grid infrastructure. The middleware solutions are not tailored to any problem, and require a significant knowledge of the inner workings of the Grid in order to use them correctly. The mechanism to define tasks and deploy them in a Grid-enabled infrastructure will require the management of authentication certificates, which is a huge overhead in order to deploy applications. This overhead is mitigated in huge projects like CERN, but in small to medium research laboratories this can be difficult and expensive. Also the thigh bound with the framework make this solutions not portable to other computing resources, like Cloud computing or local clusters. Examples: jLite, globus, UNICORE.

5. Similar lightweight tools

Several tools exists to help administrators deal with deployment and configuration in several machines via a single ssh connections. These solutions are very lightweight, because they only need an ssh connection to connect with the computational resource. Here there are different orientations regarding the nature of each tool. Some are oriented to adminsitrators, to facilitate the configuration of machines, not to deploy long-running tasks in the underlying job scheduler. Other solutions are more similar to our approach, but they only run in private resources, as a service to the customer. Examples: dispy, command.io, Celery

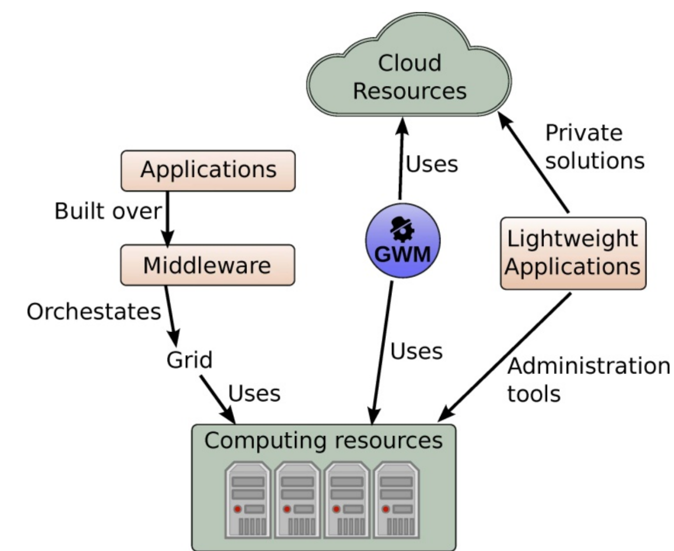

Fig. 1.General description.

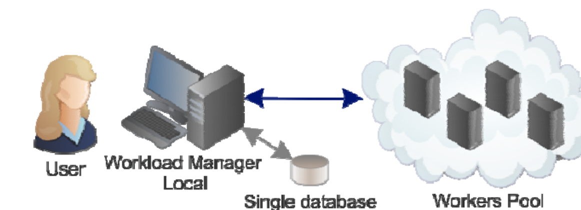

Fig. 2. Local mode of operation with the database stored in the user computer.

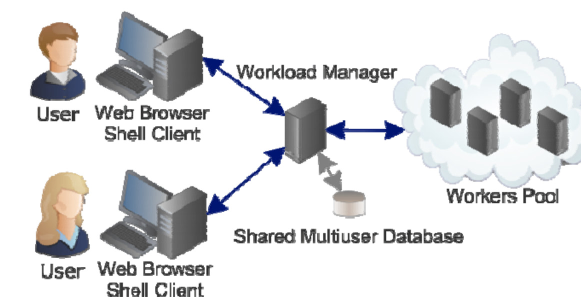

Fig. 3. Server mode of operation with the database stored in the remote computer.

On the growth mechanisms of GaAs nanowires by Ga-assisted chemical beam epitaxy

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Nanowires (NWs) are one-dimensional (1D) structures which are considered to play an important role in the fabrication of near-future electronics. These nanostructures are commonly grown by using the vapor-liquid-solid (VLS) mechanism, which is probably the most common growth mechanism due to its high successful rate. VLS fundamental principle is based on the use of metal droplets to assist or nucleate the NW growth along preferential directions determined by the substrate orientation. The metal droplet, also called catalyst, is usually in liquid phase during the growth process, acting as a sink for the growth species; once the droplet alloy becomes supersaturated, growth takes place at the droplet-substrate interface by reaction of species, accumulating enough strain to enable the coherent growth of the NW and then lifting up the catalyst.

In the particular case of GaAs NWs, Au is commonly used to assist NW growth in techniques such as metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) or chemical beam epitaxy (CBE). However, Au is confirmed to unintentionally contaminate GaAs structure, hindering its electrical properties. In order to avoid these drawbacks, Ga is proposed as the alternative for Au, giving rise to the process called Ga-assisted VLS; as a self-assisted process, it inhibits the risk of doping. The Ga-assisted VLS growth is possible due to the formation of Ga droplets in the same growth chamber prior to the NW growth, as it has been successfully carried out in previous MBE and CBE based works [1,2]. This type of growth is always linked to the existence of a SiO_x capping layer atop the substrate surface because of both, the high diffusion length of Ga atoms over the oxide layer, and the existence of pinholes where Ga droplets can be accommodated. Although this method has been proven in MBE, to our knowledge there were no reported works in the literature for techniques using metalorganic sources such as MOCVD or CBE. This may be related to the lack of metalorganic precursors able to thermally decompose on a substrate surface covered by a thick SiO_2 layer. In Ga-assisted MBE, both Ga and As atoms directly impinge on the catalyst either from the molecular beam or by diffusion from the substrate surface neighborhood. However, the CBE scenario is slightly different, because the Ga precursor needs to be thermally dissociated on the surface of the sample to later diffuse Ga along the NW facets towards the catalyst. In order to fully exploit NWs properties for advanced nanotechnology, it is crucial to understand the mechanisms governing the NW growth as well as to clarify the optimum growth conditions that will yield reproducible and consistent ways to grow NWs by CBE technique.

In this work, GaAs NWs were grown by Ga-assisted CBE on Si(111) substrates. We investigate the influence of substrate surface preparation as well as growth conditions such as V/III flux ratio, substrate temperature (T_s), growth time and catalyst dimensions on the resultant NW properties.

The successful self-formation of Ga droplets from the metalorganic precursor triethylgallium at Si oxide pinholes is demonstrated by scanning electron microscopy (SEM). The formation of these droplets is proven to enable the catalytic growth of NWs whose morphology is analyzed *ex-situ* by SEM (Figure 1), showing a self-organized array of vertically aligned match-shape GaAs NWs with a maximum length of 4 µm and a hexagonal footprint. In addition, the crystalline structure of NWs is monitored *in-situ* by reflection high energy diffraction (RHEED), showing pure zincblende phase along the whole NW stem (Figure 2). In terms of better NW aspect ratio and faster growth rates, the best growth conditions are found to be T_s = 580 ºC and an effective V/III flux ratio close to 1.

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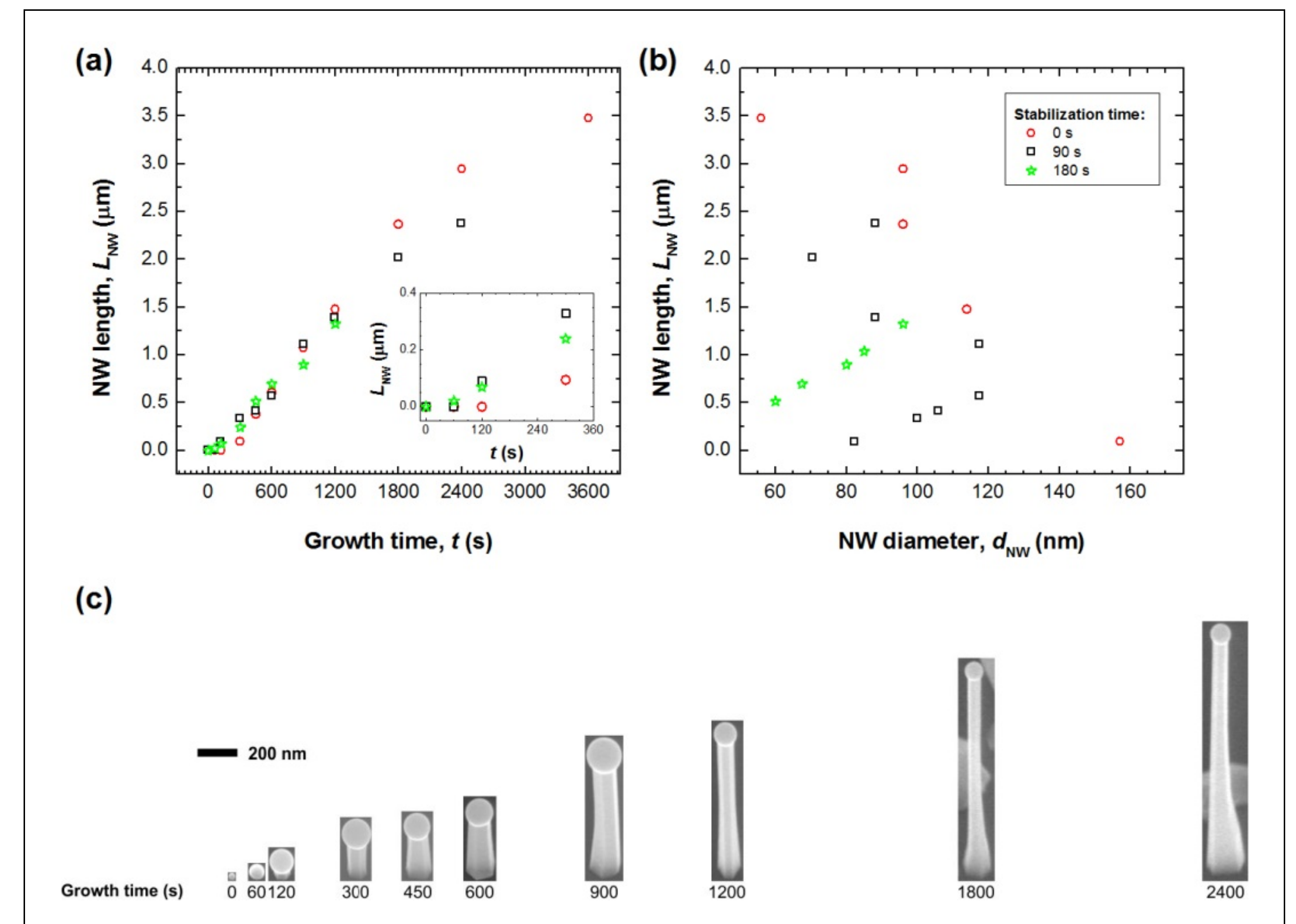

Fig.1. NW length represented as a function of (a) growth time and (b) NW diameter. Data are extracted from SEM pictures (c). Inset of (a) shows a zoom-up for low growth times.

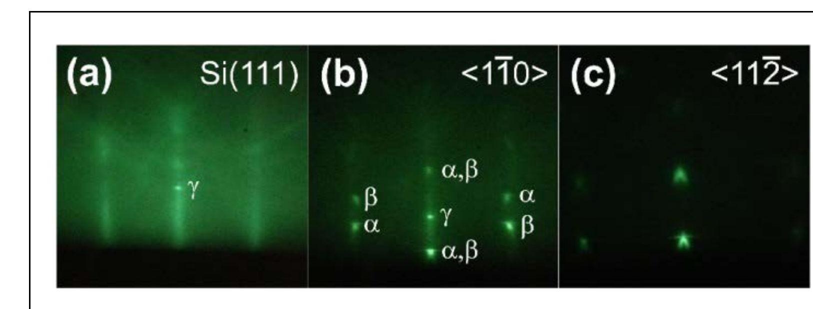

Fig.2. RHEED patterns monitored along the NW growth process. (a) Characteristic streaky Si(111) pattern observed prior to NW growth. Spotty patterns observed along (b) <1-10> and (c) <11-2> azimuths which are associated to the formation of zincblende GaAs NWs.

XPS and SEM as diagnosis tools for failure analysis after reliability tests performed on III-V multijunction solar cells

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1. Introduction

The knowledge of the behaviour along the whole working life of III-V concentrator solar cells is a basic issue which is still in its first stages. Acelerated life tests (ALT), where the stress parameter was the temperature [1], were conducted on a battery of commercial III-V solar cells. The reliability study from the data obtained was presented in [1]. In this contribution, we aim to show how typical materials characterisation techniques, namely, X-ray photoelectron spectroscopy (XPS) and scanning electron microscopy (SEM), are able to provide a rather quick and meaningful answer in the next step of the study, the failure analysis.

2. Experimental

Details about the steps followed to carry out the ALT can be found in [1]. Very briefly, solar cells were placed inside climatic chambers and subjected to current injection in darkness. The ALT took place at three different temperatures (119 ^{o}C, 126 ^{o}C and 164 ^{o}C), hereafter named as low (LT), medium (MT) and high temperature (HT), respectively. Reference samples, i.e. solar cells inside the climatic chambers without current injection, have been also included in this study.

XPS measurements were made in a Thermo Scientific Multilab 2000 spectrometer. Survey spectra and detailed core level spectra were recorded. The core level spectra were fitted using the XPSPeak software package [2].

SEM images were taken using an Helios Nanolab 650 dual microscope from FEI. Different areas of the cell structure were analyzed by preparing cross-sections using FIB milling. We have also carried out energy dispersive analysis (EDAX), in order to discern the composition of each region.

3. Results and discussion

Figure 1 (top) shows how non-degraded cells look like. EDX analyses on several points identify the composition of the antireflection coating (ARC) (1, 3, 4, 7, 8), the fingers (9) and the bus bar (2, 5, 6) (Fig. 1 bottom). From this information, it is easy to deduce that the ARC is composed of TiO_x and Al_2O_x, and the cell surface metallization consists of Au and Ag. XPS analysis on the bus bar area confirms this last point, being metallic Ag, mixed with Ag sulfide (Fig. 2 top), the main constituent.

After ALT, the solar cells are degraded and the bus bar experiencies an evolution on its chemical composition and structure. Ag oxidizes (Fig. 2 bottom left) and Ge is now present in the bus bar surface (Fig. 2 bottom right). This chemical evolution is accompanied by a noticeable degradation of the bus bar metallization (Fig. 3 bottom), irrespective of the climatic chamber temperature. The bus bar has raised up showing the two metallization stages, the electrochemically grown silver and the thin evaporated layer one. Obviously, the electric contact between bus bar and cell surface is lost in these areas.

However, there are some differences between the cells degraded at LT and HT and those degraded inside the HT climatic chamber. The last ones exhibit solder residues which probably had migrated from the space between the bus bar and the external tab, to the cell perimeter (Fig. 4 top). The cells degraded at LT and MT show cracks in their surfaces that propagate along the whole thickness of the cell structure (Fig. 4 bottom). The cracks could be due to a mechanical stress suffered by the different thermal expansion coefficients of metal and semiconductor [3]. These features are absent in the cells degraded at HT. The observed differences suggest different failure mechanisms, depending on the climatic chamber where the solar cells are degraded.

SEM and XPS have revealed as very powerful tools for the failure analysis after ALT performed on III-V solar cells. Data analysis would provide information on the failure mechanisms and on the ALT parameters suitability for these specific devices. The evolution on the bus bar chemical composition would lead to a mechanical stress that finally results in a semiconductor structure break for the cells degraded at LT and MT. On the other hand, cells in the HT climatic chamber would not get to this degradation stage, since probably, solder residues diffusion due to an excessive test temperature would cause a fatal short-circuit.

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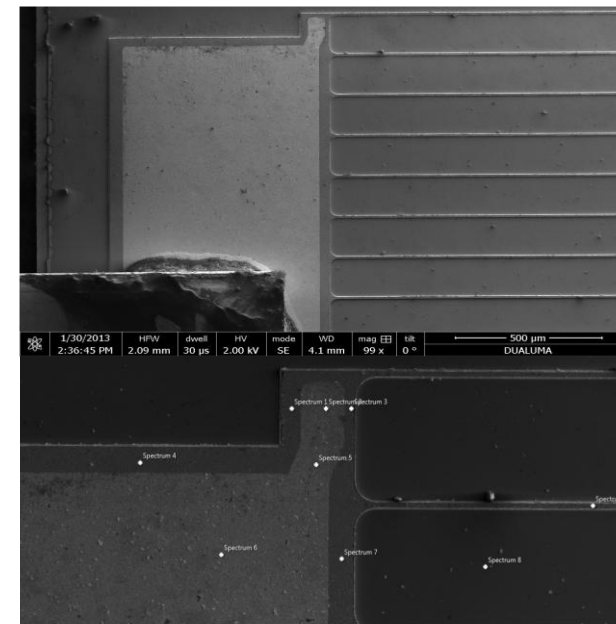

Spectrum Label	C	O	Al	P	Ti	Ga	Ge	Ag	In	Au
Spectrum 1	11.35	55.41	5.24		3.46			5.16		19.38
Spectrum 2	20.24							36.50		43.27
Spectrum 3	11.86	52.34	4.99		3.22			11.80		15.79
Spectrum 4	5.74	57.26	4.99		3.21			19.07		9.73
Spectrum 5	43.44							19.00		37.56
Spectrum 6	25.35							40.69		33.96
Spectrum 7	10.14	54.28	5.35		3.57			4.36		22.30
Spectrum 8	7.13	40.64	4.84	22.43	2.16	10.59	0.00		12.21	
Spectrum 9	15.31	51.93	4.99		3.16	0.00		7.83		16.77

Fig. 1: Top: planar partial view of a corner of a non-degraded cell showing the bus bar and the tab for external connection, and fingers. Bottom: EDX analysis in several selected points showing atomic surface composition.

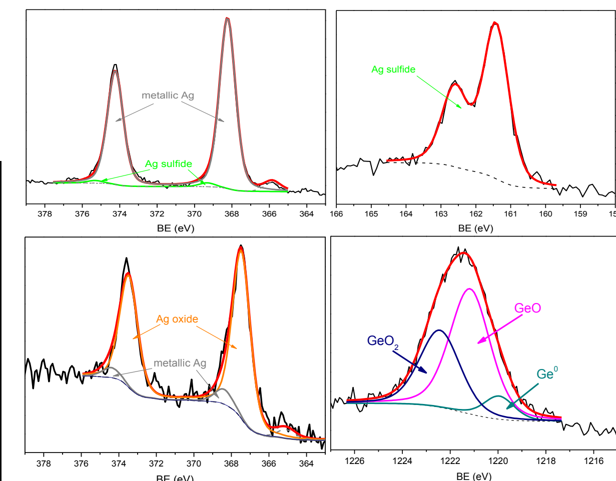

Fig. 2: (Top) XPS analysis of the non-degraded bus bar: left, Ag3d core level deconvolution; right, S2p deconvolution. (Bottom) XPS analysis the bus bar after degradation: left, Ag3d core level deconvolution; right, Ge2p deconvolution. Identification of the signal constituents is made on the figures.

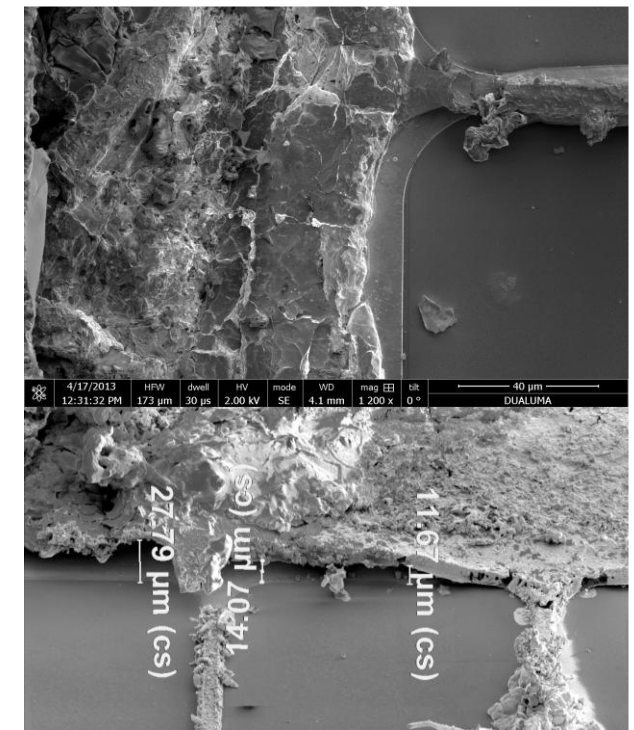

Fig. 3: Top: planar view of a damaged bus bar. Bottom: tilted view showing the detached front metallization.

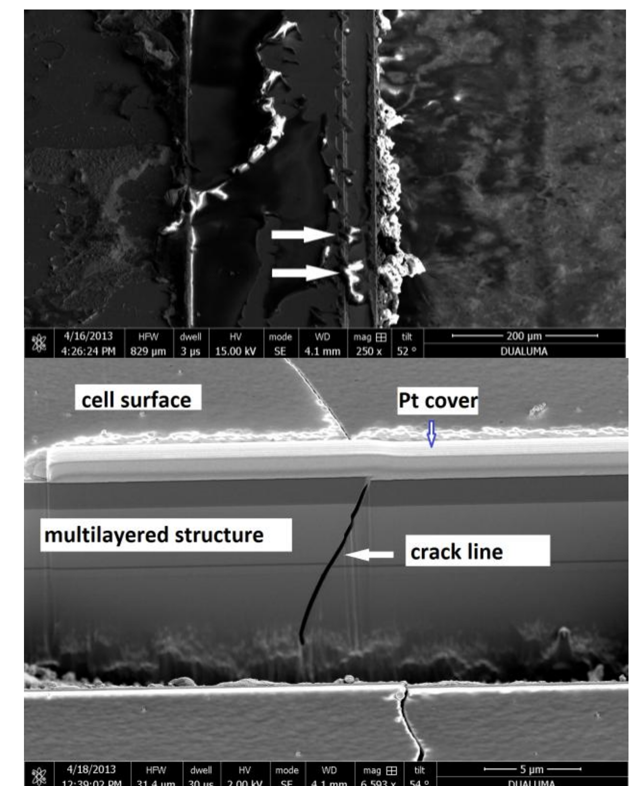

Fig. 4: Top: high temperature degraded cell structure lateral section where solder residues (white arrows) appear after degradation. Bottom: bathtub in a medium temperature degraded cell where the cracks seen in the cell surface propagate through the semiconductor structure.

Automatic transfer of graphene and its electrical characterization

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1. Abstract

Graphene has proved to be an excellent material for high-speed electronics, mainly due to its large mobility at room temperature. Among several techniques available for obtaining graphene for electronics, chemical vapor deposition (CVD) on a metal foil is the most extended one, as it provides large-area and high-quality material. This method also enables the fabrication of graphene field-effect transistor (GFET) using a planar process. In order to fabricate GFET, graphene has to be transferred from the initial growth substrate (typically copper) to a dielectric substrate, such as silicon dioxide or hexagonal boron nitride.

In this work, we focus on the optimization of graphene field-effect transistor (GFET) processing technique through an automatic transfer system. Also, a first principle model is applied for checking the GFET performance and the material intrinsic physical properties, extracting relevant information from the process itself.

2. Graphene transfer

Although there exist methods to transfer graphene automatically [1], none of them is focused on transferring to rigid substrates. Here we report an automatic, lab-sized system that can be used for this purpose.

For the graphene transfer, a copper foil with a CVD graphene layer on top is used. A thin film of PMMA is spin coated on top of it as a protective layer. Then, the sample is introduced into the system. A special PTFE container is used for centering the graphene, holding the final rigid substrate and avoiding structural damage during the process. Then a microcontroller changes the temperature and the liquid flow as depicted in Fig. 1. Finally, the sample is ready for the next processing step.

3. Electrical characterization

Some of graphene models are based strongly on solid state physics [2], whereas others are more focused on silicon FET devices [3]. The model used in this work, described in [4], is based on first principles calculations. Experimental I_{DS} vs. V_{GS} are fitted to the model. All the relevant parameters, such as the oxide capacitance (C_{ox}), voltage applied (V_{DS}) and geometry (L_g and W), among others are introduced into the model. In our case, we work with the transconductance (g_m), in order to extract some fundamental values from its shape, such as the maximum and minimum, the Dirac point, or the curve slope in several voltage ranges. Using these g_m features, the electron mobility, the total serial resistance and the total density of fixed charge are obtained. In Fig.2 the fitting result is shown for one automatically-transferred device. Finally, an experiment was performed to compare manual and automatic transferred samples, showing the latter ones the best electronic properties.

Acknowledgements
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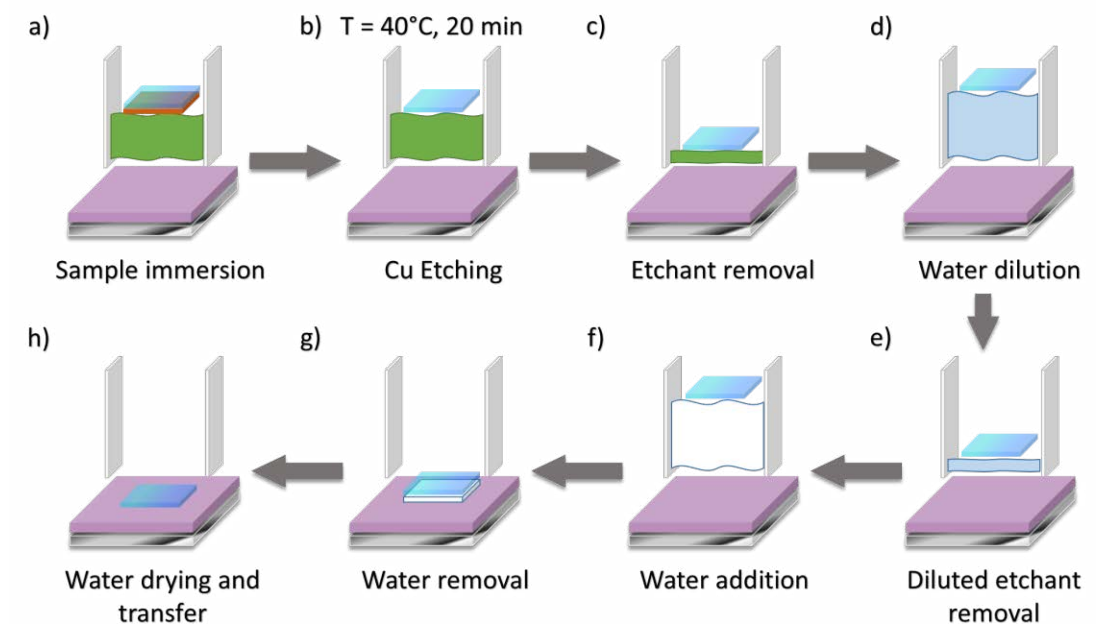

Fig.1. Scheme for the automatic transfer process. In a) the sample is immersed in Cu etchant, in b) the required temperature for the etch process is set. In c) - f) the etchant solution is gradually removed and diluted in water. In g) and h) all the liquid is removed and the sample is transferred to the final substrate.

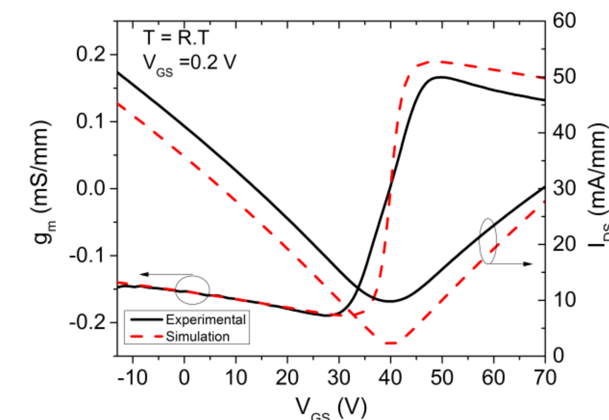

Fig.2. Transconductance (left axis) and I_{DS} (right axis) vs. V_{GS} experimental and simulated curves for a GFET using automatic transfer.

Thermal stability study of AlGaN/GaN MOS-HEMTs using Gd_2O_3 as gate dielectric fabricated on Si

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1. Motivation and Objectives

AlGaN/GaN-based high electron mobility transistors (HEMTs) are potential devices in high power and high frequency applications [1, 2]. However, high gate leakage current is one of the issues which need to be solved to improve their reliability [3]. Metal–oxide–semiconductor HEMTs (MOSHEMTs) with thin dielectric layers, such as Al_2O_3 [4], HfO_2 [5] and Gd_2O_3 [6], deposited between gate and barrier layer, have been studied as one of the solutions to reduce the high gate leakage current problem. Gd_2O_3 might be a promising candidate for the gate dielectrics on GaN due to its high dielectric constant, low electrical leakage currents and reduced interfacial density of states (D_{it}) with GaN [6]. Previous publications have shown the use of Gd_2O_3 grown by electron-beam heating [6] or molecular beam epitaxy (MBE) [7] on GaN or AlGaN/GaN structures, but there has been very little work on the thermal stability study of Gd_2O_3-AlGaN/GaN MOS-HEMTs.

In this study, thermal stability of the conventional HEMTs and Gd_2O_3 MOS-HEMTs are discussed.

2. Experiments Details

Conventional and MOS devices (diodes and HEMTs) were processed simultaneously on AlGaN/GaN heterostructure grown on Si substrate. In the MOS-HEMTs a thin layer of Gd_2O_3 was deposited by high pressure sputtering technique [8, 9] under the gate. The Gd_2O_3 layer was 4.2 ± 0.3 nm in thickness and 2.1 nm in root mean square (RMS).

I-V and pulse characterization were carried out, with the conditions shown in Table 1.

3. Results and discussion

Gate leakage current of the diodes (Fig.1) showed that reverse gate current in MOS-diodes was much smaller (3-4 orders of magnitude) than in Schottky diodes through all the process. An abrupt increase in forward leakage current in Schottky diodes was observed after 24 hours' storages at 500°C, indicating permanent device degradation in the device, in contrast to the MOS-diodes.

The transconductance of the devices has also been recorded (Fig. 2a). A positive shift of threshold voltage in MOS-HEMTs was observed: from -6.8 V for the as fabricated devices, to -5.8 V after thermal annealing, then to -4.8 V after the thermal cycle. It stabilized at -4.8 V afterwards during the thermal storage process (Fig. 2b). Thus, thermal annealing would be necessary after the Gd_2O_3 deposition.

A significant decrease (~75%) in maximum transconductance at V_{GS}=0.1 V in the conventional HEMTs after 24 hours' storage at 500°C was observed (Fig. 2a). This proved a degradation of the device, which is consistent with the degradation previously observed in the Schottky diodes.

The maximum transconductance in the MOS-HEMTs was about 40% higher than in the conventional HEMTs during the thermal storage process (Fig. 2b); this shows that MOS-HEMTs show better endurance towards high temperature than HEMTs.

Finally, some physical damage was observed in the gate metal of the devices during the last check after 172 hours' tests on both devices.

In summary, AlGaN/GaN HEMTs with a thin Gd_2O_3 gate dielectric have shown both a significant reduction in the gate leakage current and a better thermal stability than the conventional HEMTs, especially after a soft annealing.

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Process	Temperature	Time	Characterization
#1	500°C	5 mins	Before/after
#2	RT to 425°C (step 100 °C) then to RT	40 mins/step	Before/during/after
#3	500°C	8 days	Before and after 24 hours

Table.1. Measurements process in the study

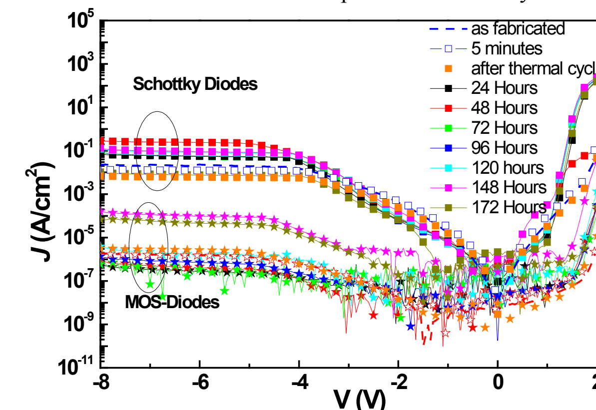
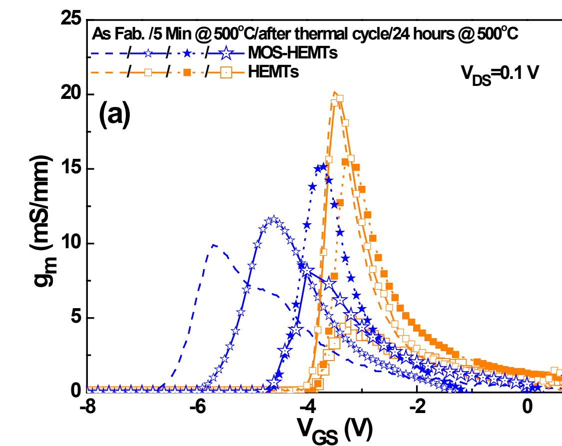


Fig.1. Gate leakage current of Gd_2O_3 based MOS-Diodes and Schottky Diodes



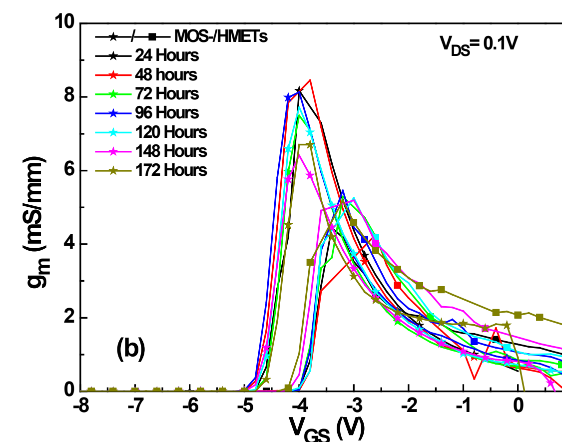


Fig.2. Transconductance characteristics of AlGaN/GaN conventional HEMTs and Gd_2O_3-AlGaN/GaN MOS-HEMTs at V_{GS}=0.1 V from process #1, #2, the first check of process #3 (a), and process #3 (b)

New Generation Architectures in III-V Multijunction Solar Cells for Efficiencies of 50%

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1. Introduction

Concentrator photovoltaic solar energy is capable of achieving electricity prices around c€3/kWh in areas with enough direct solar radiation such as Southern Europe. Most commercial concentrator systems use lattice-matched GaInP/Ga(In)As/Ge triple-junction solar cells, which show efficiencies of 38-40% (see figure 1).
Solar cell efficiency is a key factor in reducing the cost of the concentrator system and that of the GaInP/Ga(In)As/Ge triple-junction solar cell cannot be increased significantly above 40% due to intrinsic design limitations. This is the reason why novel architectures have been developed in recent years, approaching efficiencies of 45% at laboratory level [1]. Despite their potential to achieve high efficiencies, each of architectures presents a set of distinct uncertainties about their cost, manufacturability, reliability, etc. For this reason, none of these technologies is clearly ahead of the rest. Moreover, each architecture is developed by different research centers and photovoltaic companies, giving rise to a conflict of interest which leads to a lack of consensus about which architecture is the most promising one. Thus, an objective review, which has not been done, is compulsory to guide future developments.
On the other hand, the Solar Energy Institute of the Technical University of Madrid has already achieved a lattice-matched GaInP/Ga(In)As/Ge triple-junction solar cell with an efficiency of almost 40% [2]. Therefore, we are now on the way to determine the best architecture to focus on our research in the following years. Accordingly, this manuscript presents the preliminary review of the comparison among the new architectures.

2. New Generation Architectures

The four most significant architectures are the upright metamorphic (UMM), the inverted metamorphic (IMM), and the architectures based on the use of diluted nitrides and the wafer bonding. They are sketched in figure 2 and their main characteristics are:
-Upright Metamorphic: it looks for a better exploitation of the solar spectrum without the constraint of the lattice- matched epitaxial growth. A gradual buffer layer is required in order to adapt the GaInAs middle cell lattice constant to that of the germanium substrate. That is the reason why this architecture is called lattice-mismatched or metamorphic. It is being developed by Fraunhofer Institute and Azur Space in Germany.
-Inverted Metamorphic: two lattice-matched subcells are grown on a substrate followed by the metamorphic growth of the third (or more) junction(s). After that, the structure is flip chip, attached to a mechanical carrier and the semiconductor substrate is etched. So, light impinges the first subcell grown on the semiconductor substrate. It is being developed by NREL (USA), Emcore (USA) and Sharp (Japan).
- Dilute nitrides cell: it is a lattice-matched structure where one of the subcells is made up of a dilute nitride such as GaInNAsSb or GaNAsSb. Up to now, it has been successfully grown only by using MBE (Molecular Beam Epitaxy), which has a very low throughput. It is being developed by Solar Junction (USA), IQE (UK).
- Wafer bonded cell: two multijunction structures are grown separately on two semiconductor substrates. Then the two structures are wafer bonded and one of the substrates is etched back. Therefore, it is has a great potential for achieving 4 or more subcells. This architecture is being developed by Fraunhofer Institute (Germany), SOITEC (France), Spectrolab (USA).

3. Comparison Procedure

In the final paper, we will present a state of the art review of the four architectures including their main pros and cons. Besides, we will describe the procedure (solar cell manufacturing, characterization, device simulations, cost calculations, etc) we will follow in the future to select the best architecture. The goal is to respond the following questions: a) which architecture has the highest realistic potential for achieving 50% efficiencies, b) which one is the most reliable for life times higher than 30 years c) which one is the most cost competitive if they were mass-produced.

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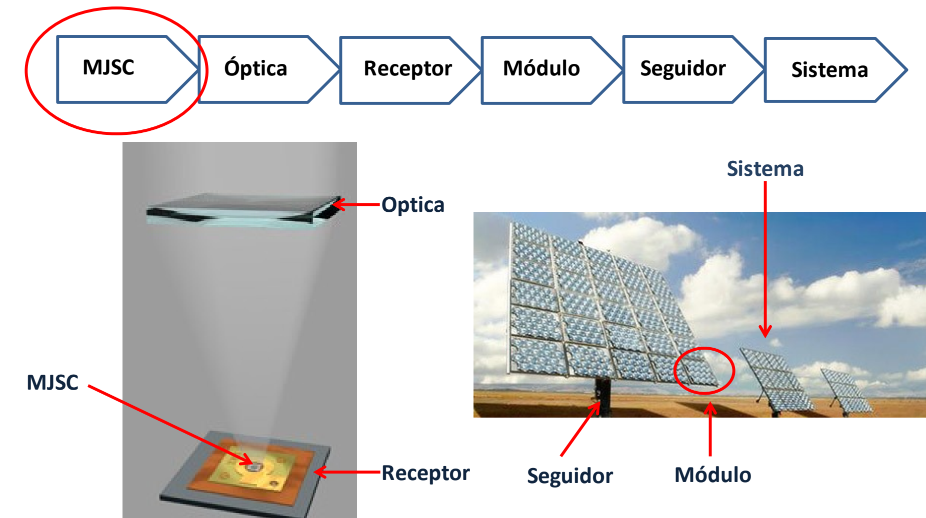

Figure 1. Elements of Concentrator Photovoltaic System. The Multijunction Solar Cell (MJSC) is the core of this technology.

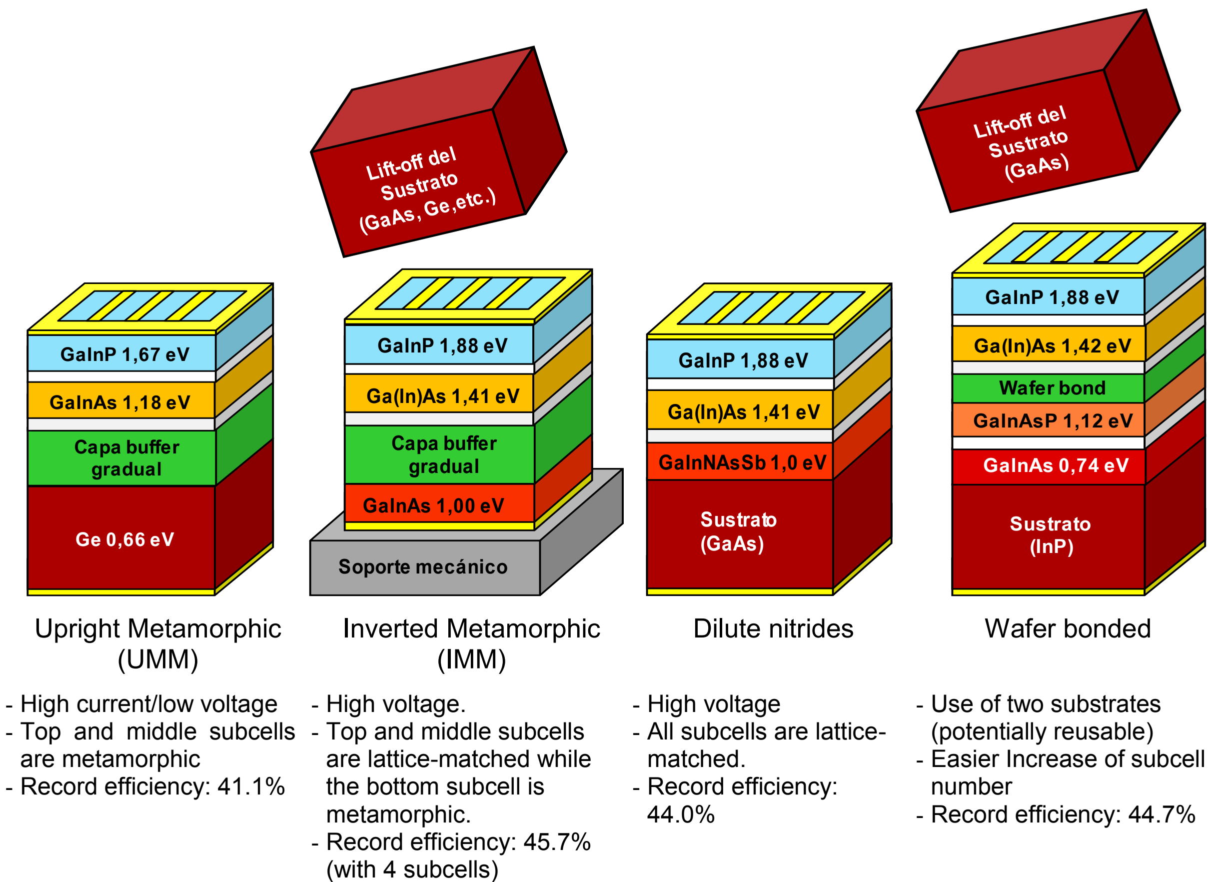

Figure 2. Schematic of the four architectures analyzed in this paper together with their main characteristics. White layers represent the tunnel junctions. For the sake of simplicity, the semiconductor substrates on which the epitaxial growths take place have the same reddish colour in spite they can represent different semiconductors at each architecture.

New result for Optical OFDM in Code Division Multiple Access systems using direct detection

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1. Abstract

In optical communication systems, OFDM has received increased attention as a means to overcome various limitations of optical transmission systems such as modal dispersion, relative intensity noise, chromatic dispersion, polarization mode dispersion and self-phase modulation. The multipath dispersion limits the maximum transmission data rates. In this paper we investigate OFDM system where multipath induced intersymbol interference (ISI) is reduced and we increase the number of users by combining OFDM system with OCDMA system using direct detection Incorporate OOC (orthogonal optical code) for minimize a bit error rate.

Keywords—*OFDM , OCDMA , OOC (orthogonal optical code) , (ISI) , prim codes (Pc).*

2. INTRODUCTION

The demand for a wireless broadband communication link capable of supporting multimedia applications at high data rates is growing. The existing RF and wired based technologies available (such as Wi-Fi, WiMax and WLAN) suffer from the bandwidth bottleneck but offer mobility and flexibility. In number of applications where higher data throughputs is more of requirement than the mobility, transmission link based on optical wireless would be one of the best options as outlined in [1-4]. Recently, white LEDs have been used for both illumination and indoor wireless communications [1-4]. A number of techniques have been proposed for using Visible Light, in recent years, optical CDMA scheme has been introduced [5] to eliminate the MAI effect and preserve the orthogonality between users in the system. In OCDMA systems, the detection process affects the design of transmitters and receivers.

In general, there are two basic detection techniques namely coherent and incoherent detections. While coherent detection refers to the detection of signals with knowledge of the phase information of the carriers, incoherent detection refers to the case without such knowledge. Using coherent processing, the schemes allow the use of bipolar orthogonal codes, such as gold sequences [3], with close-to-zero cross correlation functions, thus reducing MAI. In incoherent optical signal processing, the signature code is a family of unipolar (0, 1) sequences. To reduce MAI, the signature code must be sparse in binary ones and have very low autocorrelation sidelobes and cross correlation functions [5].

The main goal of this study is to combining OFDM system with OCDMA system to improve the performance of optical network. This paper is organized as follows. In Section 2 we provide OCDMA system with direct detection, their properties. Section 3 gives an overview to OFDM system. In Section 4 we introduce our proposed design. Comparison and discussions are given in Section 5. Conclusions are drawn in Section 6.

3. OFDM SYSTEMS

In an OFDM scheme, a large number of orthogonal, overlapping, narrow band sub-channels or subcarriers, transmitted in parallel, divide the available transmission bandwidth. The separation of the subcarriers is theoretically minimal such that there is a very compact spectral utilization. The attraction of OFDM is mainly due to how the system handles the multipath interference at the receiver. Multipath generates two effects: frequency selective fading and intersymbol interference (ISI) [3].

The "flatness" perceived by a narrow-band channel overcomes the former, and modulating at a very low symbol rate, which makes the symbols much longer than the channel impulse response, diminishes the latter. Using powerful error correcting codes together with time and frequency interleaving yields even more robustness against frequency selective fading, and the insertion of an extra guard interval between consecutive OFDM symbols can reduce the effects of ISI even more [4]. Thus, an equalizer in the receiver is not necessary.

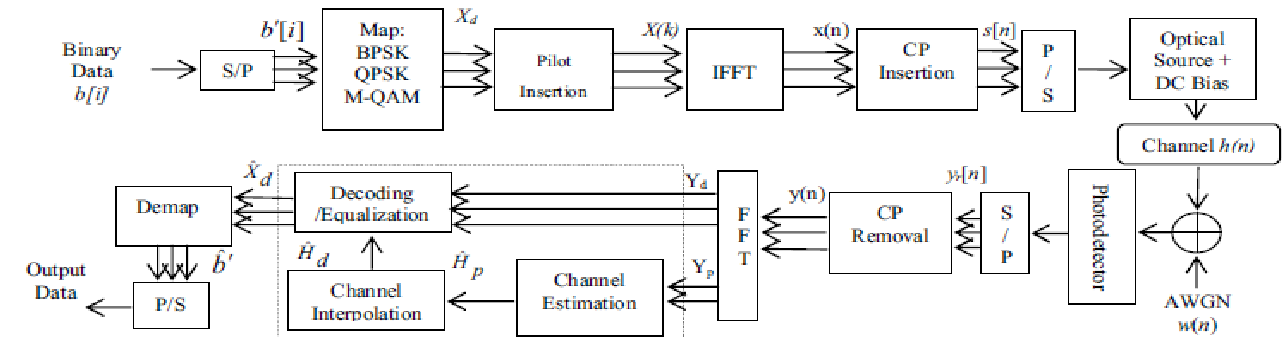

Fig.1 OFDM transmitter and receiver [4].

The Baseband model of an optical OFDM transmission system is depicted in Fig. 1. An input binary bit stream b[i] is grouped by passed through a serial-to-parallel (S/P) converter to generate parallel streams before being modulated. Here the modulation schemes adopted are the BPSK, QPSK, and M-QAM.

4. OCDMA SYSTEM WITH DIRECT DETECTION

In general, there are two basic detection techniques, namely coherent and incoherent [5-8].Coherent system uses bipolar code words whereas incoherent system consists of unipolar sequences in the signature code. Incoherent detection has a less hardware complexity compared to coherent detection because it does not need phase synchronization. In this study, the incoherent detection using direct techniques is used. Fig. 2 illustrates the block diagram for incoherent OCDMA system with direct detection.

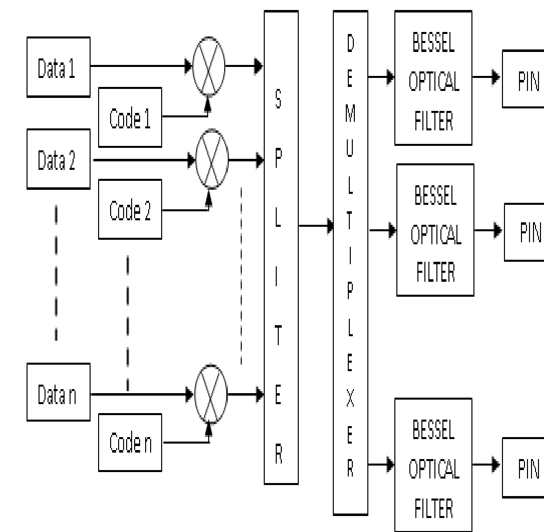

Fig. 2 block diagram for incoherent OCDMA system with direct detection.

5. PROPOSED DESIGN

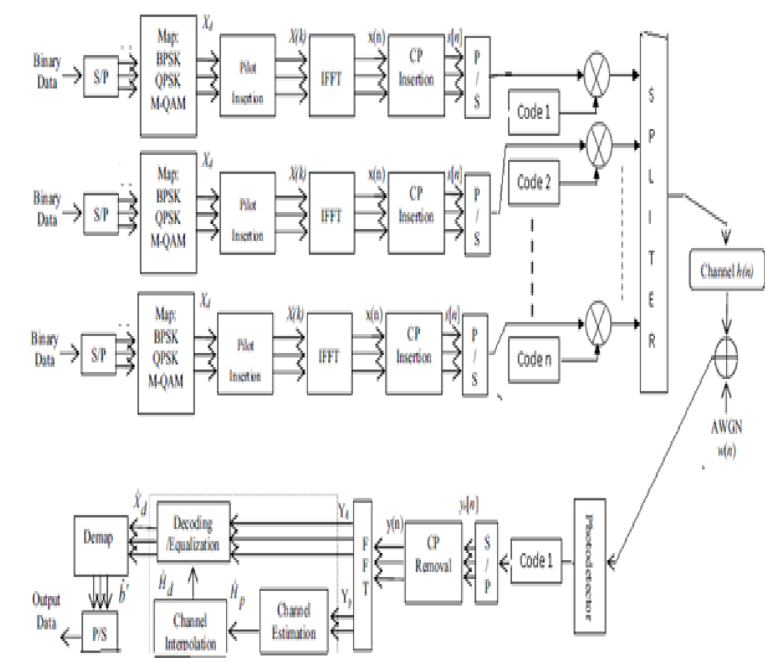

Fig. 3 block diagram for proposed system with direct detection.

The transmitted information symbols X(k) are the frequency coefficients and the output of the IFFT stage x(n) is the time domain of the input samples: x(n)= IFFT {X (k)}(n), where n and k = 0, 1, 2, …, N-1. In optical system with intensity modulation, only real-value and positive signals are used, therefore in OFDM, the subcarriers should have Hermitian symmetry to produce real value. To mitigate the effects of multipath induced ISI, OFDM symbol is preceded by a guard interval of G-sample (or cyclic prefix (CP) as shown in Fig. 3 The length of G-sample depends on the channel delay spread and is normally considered to be grater than or equal to the channel length (impulse response time) to ensure prevent ISI, the OFDM signal is passed through a parallel-to-serial converter (P/S), Finally, the signal of each users is passed through an optical modulator converter the electrical signal to an optical signal, the signals of all users are summed.

6. Performance analysis and simulation

The performance analysis of proposed system was simulated by the MATLAB. Fig.2. In the present case the number of active user is variable and the code's weight is W=3. The proposed scheme is simulated with the following conditions. Optical sources used are four sets of white light LEDs located at a height of 2.5 m, dispersion of 16.75 ps/nm-km and non-linear effects such as four wave mixing and self phase modulation were activated and specified according to the typical industry values to simulate the real environment as close as possible. The noises generated at the receivers are set to be random and totally uncorrelated. Fig.3 represents the BER performance of proposed system against the signal to noise ratio.

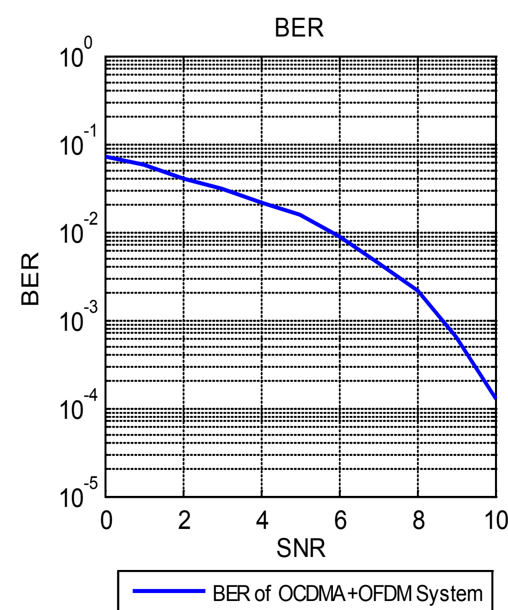

Fig. 4 BER performance for the proposed system

In Fig.4 We Showed that the proposed system is more performance that the OCDMA system, we remark the BER under 10-10 for number of users equal to 200.

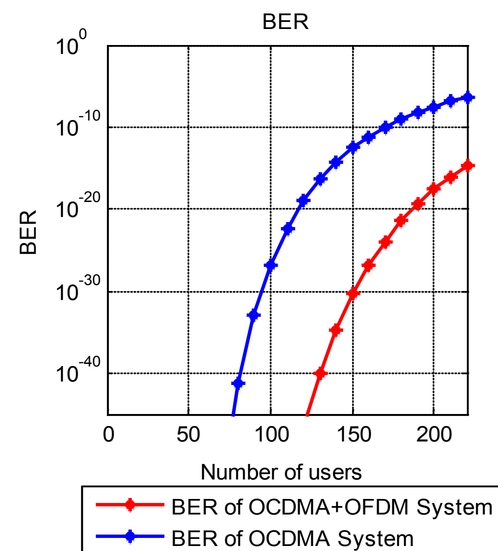

Fig. 5 BER performance comparisons for OCDMA and the proposed system

Fig. 5 shows the variations of the BER for different numbers of simultaneous, when the number of users is less than 150 users, the proposed system using direct detection will have the best performance. This is because the combining of the OFDM system. Fig. 5 also shows a better performance for the proposed system compared to OCDMA system.

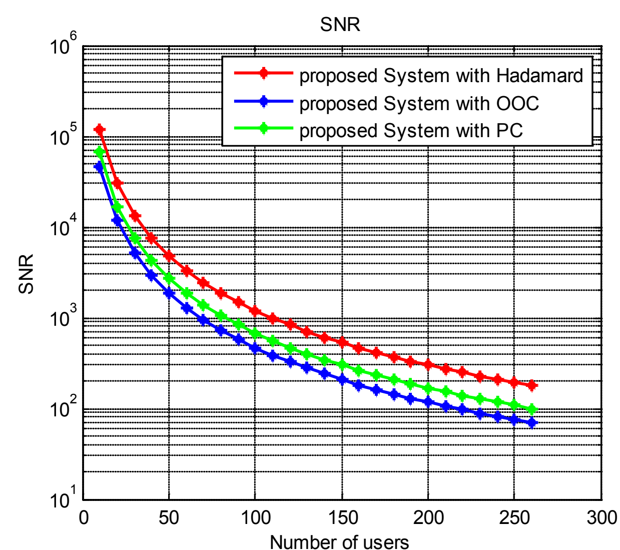

Fig. 6 BER performance for the proposed system

Note that Figure 6 shows a significantly better performance of OOC code compared to Hadamard and PC codes. The graph also shows that at typical SNR for optical communication system ranges from 10^{-3} to 10^{-2}, 100 to 200 users can be used simultaneously.

Conclusion

In this paper, we have combining the structure of OFDM with OCDMA system transmissions through optical fiber. In the absence of the MAI by the using MD code, we have shown that the BER is improved as well in a noiseless case with only thermal noise.

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Ge nanowire-based gas sensor fabricated by localized growth on microhotplates

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1. Abstract

The fabrication of germanium nanowires locally on top of a heated micromembrane with a microsized heater and interdigitated electrodes is presented. The resulting device has been tested as gas sensor towards CO, showing a stable and reproducible gas response. A possible explanation of the gas sensing mechanism is not yet clear and seems not to be the same as for metal oxides.

2. Introduction

Nanowires have emerged as important topic of research due to their high aspect ratio, and the capability to form part of new device architectures [1]. Especially monocrystalline materials are important to achieve effective and known interactions of their surface in several applications [2].
Relevant requirements appear in the use of nanoscale devices, for large scale production, as the reliability and homogeneity of their properties. Integration of nanowires or nanostructures in general into electronic and functional devices is a challenging issue because of the handicaps presented in their handling, and assembly steps.
Preparation of nanostructures based-on devices usually involves transfer of such nanostructures from the substrate where they were grown to the final device fabrication. A strategy to achieve more reliable, reproducible and less time consuming device would include the localized growth of these nanostructures in final electronic device, avoiding several steps that add uncertainties factors to process fabrication.
In this direction, here we present a direct growth of inorganic germanium nanowires on top of CMOS compatible microhotplates and micromembranes with buried heater incorporated in order to provide the thermal energy necessary to synthesize the nanowires [3].
Devices used for this purpose have an insulating layer between heaters and interdigitated electrodes, which are on the top of surface and are used as terminals to apply electrical field to the synthesized nanostructures.
A device with nanowires grown in situ has been tested as a gas sensor device, showing the potential of this technology.

3. Experimental setup

Ge NW were synthesized using a thin Au film of 2-5 nm, sputtered on top of the hotplate, which acted as a growth seed of the CVD approach. The precursor used was diphenylgermane, requiring a temperature below 675 K for the growth. Microhotplates with suspended membranes or closed membranes were used to grow Ge nanowires.
The same heater used for providing the required temperature for the growth was used for heating the grown nanowires to right operating temperature, which ranged between 323 and 393K.

4. Results and discussion

These nanowires are localized preferentially between the IDE contacts, although a coating of Au has been deposited on Pt heater top surface. HRTEM analysis showed monocrystal germanium nanowires, but surrounded by an amorphous GeO_x layer. Contrarily to silicon, germanium oxide due to oxidation in air is not stoichiometric and shows a variation of its oxygen concentration that increases from the interface Ge/GeO_x towards the nanowire surface.
Response of the Ge nanowires towards CO gas pulses at different concentrations and temperature has been tested. The results show that at 100ºC operation temperature a reproducible signal of the sensor, which is of about 2% at 10ppm of CO, but the response time is quite long, of some hours. The use of a higher temperature does not improve the results and gives rise to a drifting signal, probably because of the further oxidation of the outer GeO_x layer.
Although in metal oxide nanowires an accepted model of adsorption of the gas and charge transfer to the semiconductor body exists, the same model seems difficult for explaining the gas sensing behavior of germanium nanowires [4], due to the strongly isolating nature of GeOx, presenting a bandgap in excess to 5.5eV.[5]

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Hybrid Integration of VCSEL and Microlens for a Particle Detection Microoptical System

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1. Abstract

We introduce the design and fabrication of a microoptical system of reduced dimensions, based on hybrid integration of commercial components (ie. VCSELs and microlenses) using silicon micromachining. We demonstrate the feasibility of integration of these components and to provide up to 4 collimated or focused laser beams. The application for this system will be the detection of microparticles and to perform 4 parallel measurement.

2. Introduction

For many biological applications, it is necessary to count the amount of cells or particles found in a sample. Since 1990 the interest in LoC and µTAs biosensors has increased considerably. These devices perform fast measurements using small sample volumes (µl), providing results with good accuracy. Miniaturization and integration of optical components in LOC is an important activity. The goal is a efficient coupling and focusing of light into the window measurement, with fiber optics or the integration of optical sources as near as possible.[1,2]

In this work we present the design, fabrication and test of a miniaturized package suitable for detection of microparticles with a diameter in a range of the tens microns.

3. Optical Design

With ZEMAX, a ray tracing simulator, we determine the optimum positions and dimensions of the elements, analyzing two possible scenarios: collimated or focused light beams. In the first case, the aim is to optimize the minimum size of the spot radius of the laser beam at the position where the microfluidic channel will be placed. In the second case, collimated light, the objective is to obtain a collimated beam.

VCSELs from "ULM Photonics" emit at a wavelength of 850 nm This VCSELs are commercialized in dies forming linear arrays of 4 or 12 lasers, with a pitch of 250um. Their divergence angle is 30º (full width 1/e^2).

MicroOptics is necessary to correct this and allow the focusing or collimating of the light beams. The microsystem includes a microlenses array from "SUSS MicroOptics" (fig. 3), fabricated in fused silica material, The circular microlenses present a focal length of 1.063 mm, a radius of curvature (ROC) of 0.487mm and also a pitch of 250um.

In the focused scenario the optimum radius of laser spot at the microfluidics channel position was found when the distance VCSEL-Dectector = 24mm and the microlenses was placed at $d_{V\text{-}L} \approx 1.1$mm from the VCSEL. For those conditions, a radius spot of 136microns was obtained. The effect of a particle blocking the light is shown in the detector #2, after glass substrate. Figure 1 is a representation of of the shadow produced by a 50µm radius particle in detector position, after microfluidic channel and glass substrate.

4. Fabrication and test.

The VCSELs and the microlenses must be assembled according to the results of ZEMAX simulations. Two pieces (base and spacer) are designed and fabricated with silicon micromachining procedures. In the silicon base, a cavity must be fabricated in order to place the VCSEL. Over the base, a "U" shape spacer with 1.23mm thickness to accomplish the optical requirements of the system is placed.

Figure 2 is a photograph of the micromachined components and the final package including microlens on the top. Finally in figure 3 it is shown the good collimation of the microsystem till distances of 3cm, between VCSEL and detector, enough to put between them the microfluidic system.

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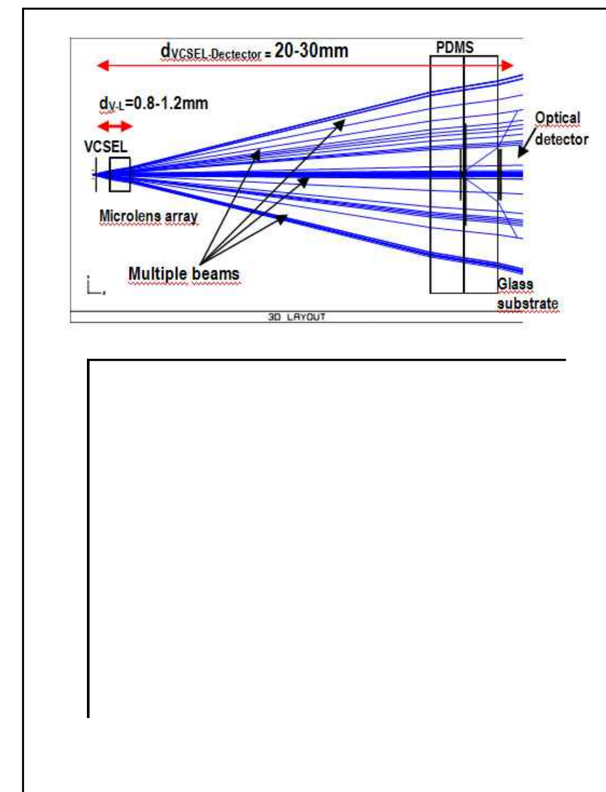

Fig.1. Top: example of design on ZEMAX software. Bottom: shadow of 50µm radius particle in the channel.

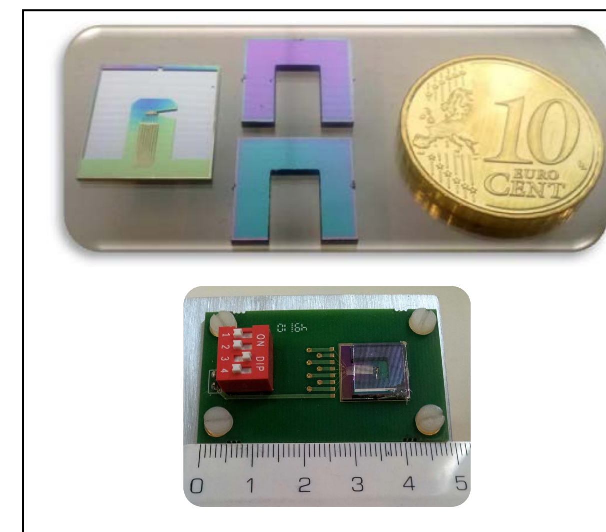

Fig.2. Top: Base with VCSEL and electrodes, and "U" spacer. Botton: Microlens array mounted on the top.

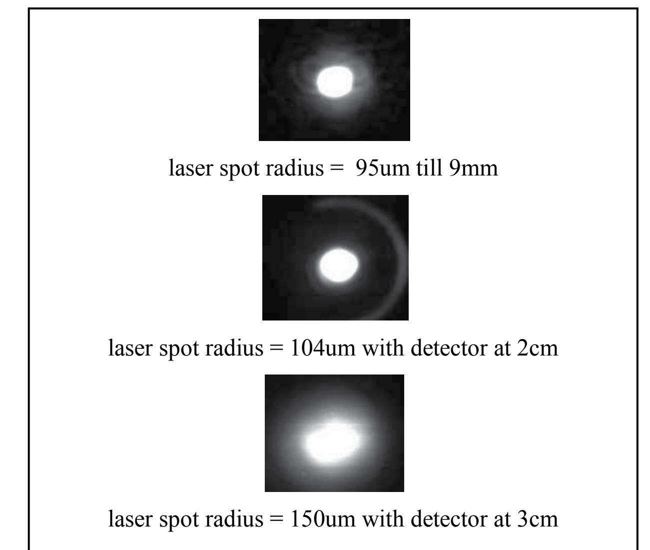

Fig.3. Measurement with a commercial camera of the radius of laser spot at different distances.

Intracellular Silicon chips:
A new research line at the IMB-CNM (CSIC)

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1. Abstract

In the last years, our group (Micro- and NanoTools group) from the IMB-CNM (CSIC) has started a new research line focused on the shrink of silicon chips to small sizes compatible with being internalized inside living cells. These devices unite the versatility of silicon MEMS to the advantages of intracellular application of the cell internalizable micro- and nanochips. This contribution tries to summarize our experience in the fabrication and collection of suspended chips from silicon microparticles (the stone age of this work) based on photolithographic process to intracellular NEMS (the nanosystems age)(Fig.1).

2. Introduction

Improvements in the fields of the micro- and nanotechnologies allow the fabrication of structures with features at the scale of living cells. Today, creative and functional silicon based MEMS are commonly used to study fundamental problems in cell Biology [1]. These devices, which have dimensions larger than cells, are used on extracellular or partially invasive applications. On the contrary, chemically synthesized micro- and nanoparticles, smaller than cells, are excellent candidates for intracellular applications. In this work we present different aspects related to a new line of biocompatible devices obtained by microfabrication techniques for intracellular single cell analysis.

3. Intracellular silicon chips

Suspended silicon microparticles (3.0 µm x 3.0 µm x 0.5 µm) were the first devices that were developed by our group (Fig.2). The first internalization tests of these particles in HeLa cells [2] were a proof of concept of the potentiality of these devices. Next step was the design and fabrication of intracellular polysilicon barcodes (Fig. 3) for cell tracking by using geometrical and optical readout (Fig. 4) [3]. More ambitious was the application of these barcodes for tagging of mouse embryos (Fig. 5) as well as bovine and human oocytes and embryos to prevent mix-ups in assisted reproduction [4]. We go one step beyong withs the fabrication of a cell internalizable NanoOptoMechanical Sytem (NOMS) (Fig. 6) [5]. The design and fabrication of a silicon chip (6.0 µm x 4.0 µm x 0.4 µm) with an integrated mechanical sensor and a Fabry-Pérot resonator as an optical transducer that can be used as an intracellular pressure sensor. The sensing principle is based on the deflection of these nanometric membranes as a function of the pressure. How to detect this deflection was the real challenge. Hence, the two polysilicon 50 nm thick membranes were separated by a vacuum gap, ~300 nm, acting as two parallel mirrors to form an optical resonator whose optical spectrum is modulated by the distance between them.
Suspended silicon microparticles, barcodes and pressure sensors were fabricated by using standard semiconductor techniques based on photolithographic processes which allowed the fabrication of millions of devices per a 4” wafer. The combination of deposited layers of polysilicion, as structural layers, and silicon oxide, as sacrificial layers, allowed the 3D structuring of the chips and their release from the wafer. Released chips were suspended in ethanol for collection.
The cell-internalization methodology used with the silicon microparticlesand barcodes was also applied with the intracellular pressure-sensor devices, allowing their internalization without affecting their structural integrity nor the cell viability. Pressure changes inside intact HeLa cells could be detected.

3. Conclusions

To sum up, we will report several crucial aspects in the way from the internalization of a silicon particle to the development of intracellular silicon NOMS: technology, chips collection and manipulation, cell internalization, cell viability, mechanical and optical considerations, measurement set-up.The possibility to shrink these devices to a scale smaller than a living cell opens endless possibilities in many fields from fundamental studies in cell biology to nanomedicine.

Acknowledgments

This work was supported by the Spanish Government grant TEC2011-29140-C03. The authors also thank the cleanroom staff of IMB-CNM for fabrication of the chips. This work has been done in collaboration with the groups of Dr. Suarez (CIB-CSIC), Dr. Pérez (UB) and Dr. Nogués (UAB).

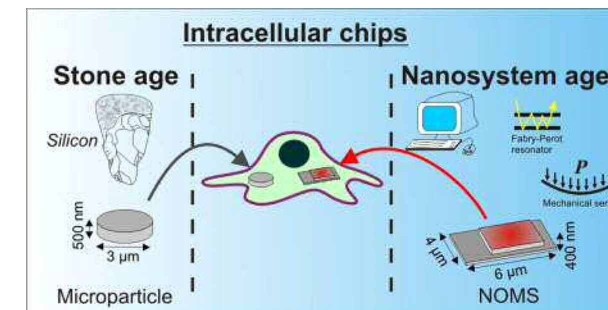

Figure 1: Schematic of the silicon microparticles and the silicon pressure sensors with integrate mechanical membranes and a Fabry-Pérot optical resonator.

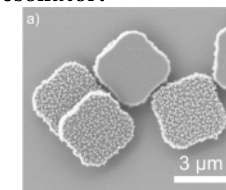

Figure 2: SEM images of the fabricated silicon microparticles

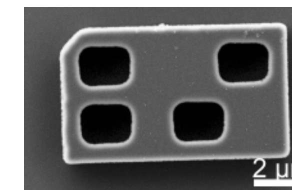

Figure 3: SEM images of the fabricated silicon barcode.

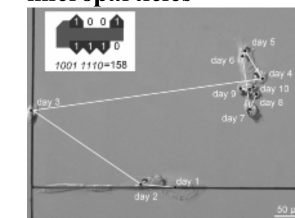

Figure 4. Daily move-ments of encoded macrophage-158 during 10 days in culture [3].

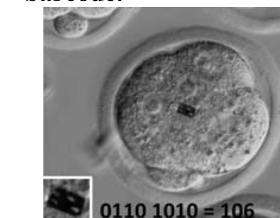

Figure 5. Tag of mouse embryos[4]

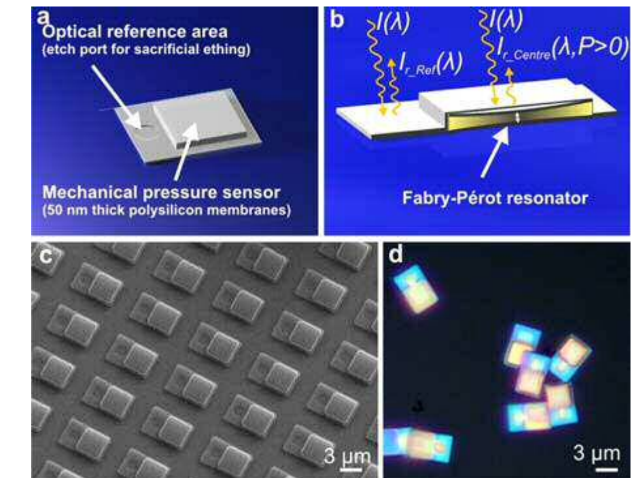

Figure 6. Intracellular pressure sensors [6].

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Chemical vapour deposition of 3D graphene foams: synthesis, properties, and applications

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1. Introduction

Graphene foams (GFs) fabricated by chemical vapour deposition (CVD) [1] provide a versatile and scalable 3-dimensional (3D) network structure retaining the outstanding properties of 2D graphene. The unique combination of high specific surface area and outstanding electrical and mechanical properties of GFs and their composites offers new possibilities in a large variety of applications including energy storage devices [2,3], sensors [4], and thermal management of electronic devices [5].

In this work, we focus on the CVD synthesis of graphene on Cu and Ni foams, the study of the graphene properties and their correlation with those of the metal template, and the fabrication of supercapacitors based on the functionalization of the free-standing GFs with conducting polymers.

2. Synthesis & characterization of GFs

GFs have been synthesized by CVD and plasma-enhanced CVD in a 4-inch Aixtron Black Magic CVD reactor. Copper and nickel foams have been are used as templates, leading to coatings ranging from monolayer graphene to ultrathin graphite depending on the selected metal and the particular CVD conditions. Figure 1 shows a general and a detail view of the GFs inspected by SEM. The properties of graphene grown by CVD are influenced by the grain structure of the metal substrates used as templates. However, despite the strong polycrystalline character of 3D metal foams, high quality graphene is obtained in these templates. Thus, Cu foams provide high quality monolayer graphene with almost no defects as indicated by the I_{2D}/I_G and I_D/I_G ratios of the Raman spectrum, Figure 2(b), not far from the Raman signature of a much less polycrystalline Cu film on a Si wafer, Figure 2(a).

3. Fabrication of GF supercapacitors

After removing the metal scaffold by chemical etching, the free-standing GFs have been functionalized by means of in-situ polymerization of conductive polymers. In particular, the GFs have been coated with polyaniline (PANI) and polypyrrole (PPY) films of different thickness and morphology. The resulting composite structures have been tested as electrodes of a supercapacitor providing excellent performance. Figures 3(a) and 3(b) show, respectively, the voltammetry and galvanostatic charge-discharge curves of a PANI/GF supercapacitor.

Acknowledgements

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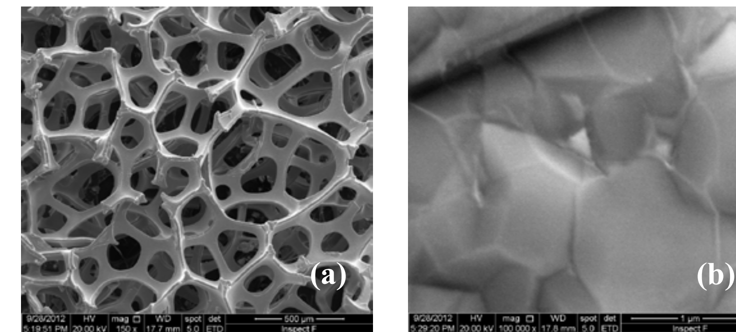

Fig.1. (a) General and (b) detail SEM images of a metal foam coated with graphene.

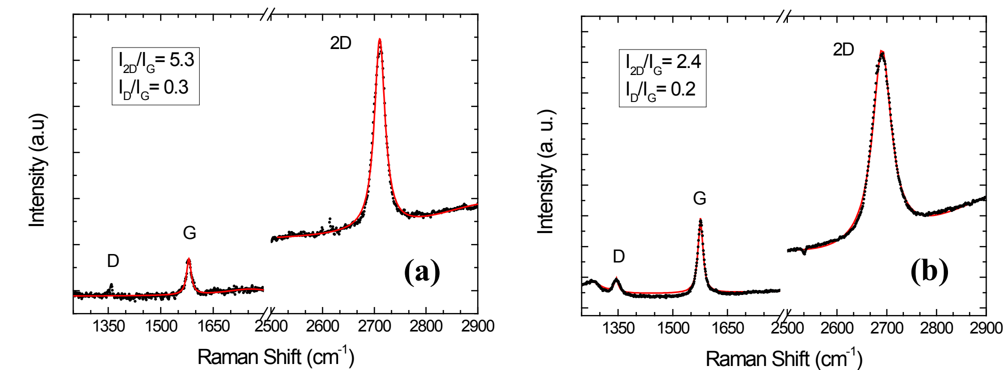

Fig.2. Raman spectra of monolayer graphene on Cu (a) film and (b) foam.

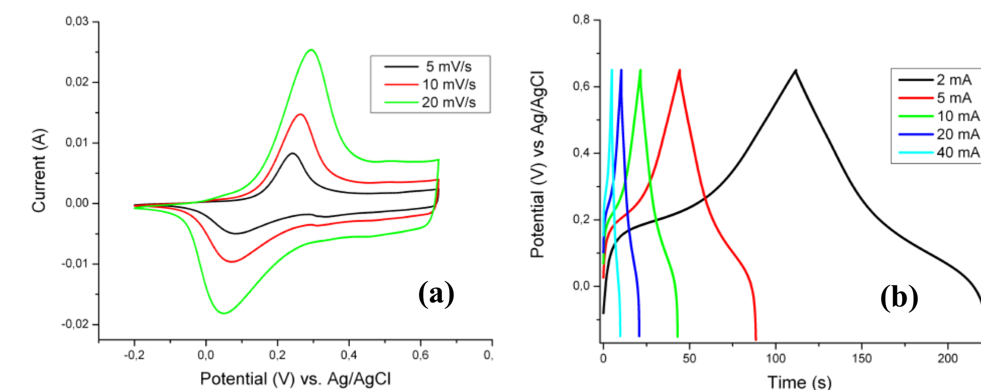

Fig.3. (a) Voltammetry and (b) galvanostatic charge-discharge curves of a PANI/GF supercapacitor.

A New Kind of Miniature Sun Sensors Design

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1. Abstract

This paper presents the design of a new type of digital sun sensors which can be applied to micro spacecraft especially micro satellites. The optical system, which adopts the CMOS APS area array sensor while abandoning the traditional way of utilizing portiforium to achieve the introduction of sun light, is different from common systems. The uniqueness of the design lies in the perpendicular double-slit structure. By windowing image reading through software settings of the sensor, we can obtain the obliquity of light relative to two axes thus calculating the actual sun light angle. Since there is no need to read the image information of the entire area array, this design can significantly increase the data updating frequency with no loss of data accuracy.

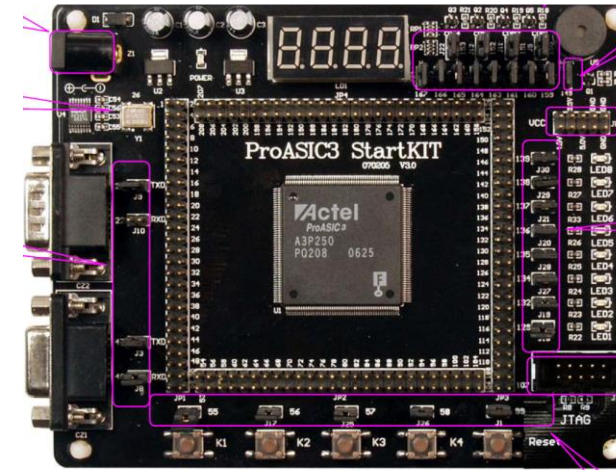

Fig.1. Flash FPGA of ACTEL(DPU)

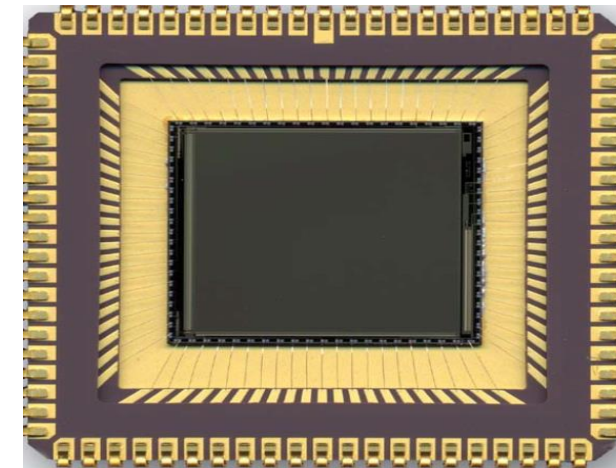

Fig.2. CMOS Image Sensor

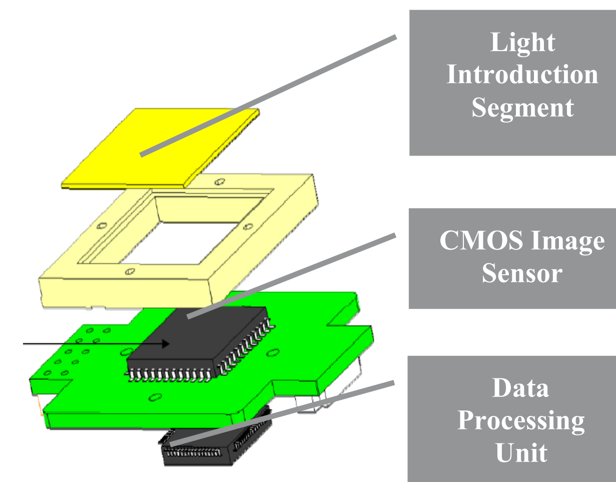

Fig.3. Simplified Sun Sensor Structure

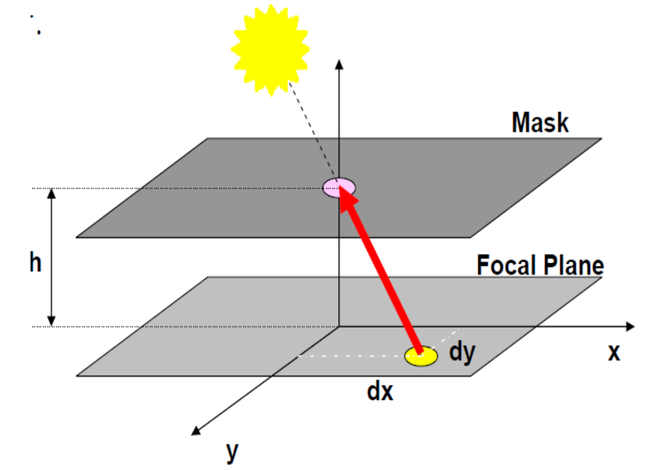

Fig.4. Diagrammatic Sketch of Optical system

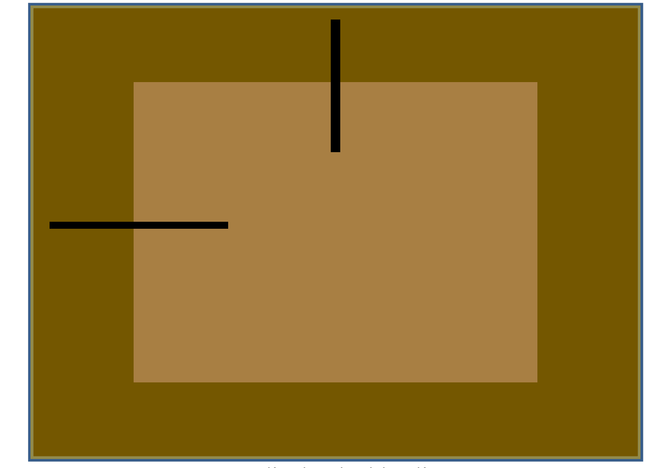

Fig.5. Perpendicular double-slit Structure

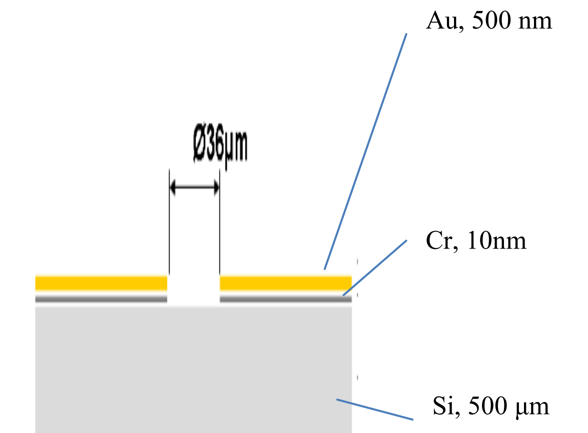

Fig.6. The Hole-Type Mask Etched by MOEMS technology

Influence of systematic gate alignment variations on static characteristics in DG-SB-MOSFETs

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1. Introduction

The substitution of the highly doped source and drain regions in traditional MOSFETs with a silicide interfacing the metallic terminal and the semiconductor gives rise to the Schottky Barrier (SB) MOSFET [1]. This structure, in conjunction with Double Gate (DG) configurations stands as a candidate to overcome some of the disadvantages of dowscaling as stated in the ITRS roadmap. However, as transistors downscale, variations occuring during its manufacture make variability an increasingly major concern.

The aim of this work is to examine the static performance of DG-SB-MOSFETs when systematic variations on the gates alignment take place by means of a particle-based 2D ensemble Monte Carlo simulator. Carrier injection through Schottky contacts, that occurs mainly by quantum tunneling, was calculated by means of the Wenzel-Kramers-Brillouin (WKB) approach. Also, the image charge effect responsible for the Schottky Barrier Lowering (SBL) is incorporated [2]. The effective potential approach is implemented in order to consider the effect of space quantization with an affordable computational cost [3].

The topology of the device taken as a reference [4] is shown in Fig. 1-a. Three misalignment scenarios were proposed [5] in order to sistematically carry out the corresponding Monte Carlo simulations:

- SGM: Single gate misalignment (Fig. 1-b)
- BGSD: Both gates in the same direction (Fig. 1-c)
- BGOD: Both gates in opposite directions (Fig. 1-d)

L_m is the misalignment lenght, that corresponds to the displacement of the upper gate in the direction of the x axis, so it is considered to be positive when it deviates to the drain and negative when it does to the source. Its considered values range from 0 to ±5 nm, so no overlap on the source or drain was taking into account.

2. Results

The influence of gate misalignment on the I_D-V_{GS} curves (Fig. 2) increases with applied gate voltage, while the threshold voltage remained almost unaltered. For the highest gate-source bias applied, current variations showed to be much more significant compared to traditional MOSFETs [5] due to the different operation principle in SB-MOSFETs.

The carrier concentration profile and therefore their injection through the source was found to be the key to explain the variations in current. The injected tunnel current to total injected current ratio (Fig. 3) shows that for $V_{GS}\geq 1$ V the majority of the injected current is due to to quantum tunneling. Moreover, it was noted that injected tunnel current alterations accounts for most of the shifts in carrier concentration, since absortion and injection components of thermionic current remains almost compensated. Quantum tunneling is modulated by the alteration of the potential profile in the regions controlled by the gates. This results in a narrower barrier when the gates are closer to the source and vice versa due to the fact to the injection is regulated by the proximity of the gate to source contact.

The carrier mean velocity and trajectory along the first 10 nm of the channel (Fig. 5), shows a net vertical flow that goes from the most populated area to the center of the channel in the vicinities of the source contacts. This effect is more noticeable in the BGOD case, where the relative misalignment between the gates is the greatest of the three scenarios.

Transconductance (Fig. 4) showed great variability with gate misalignment (up to +90%/-55%).

Regarding microscopic transport characteristics (Fig. 6), the most ballistic transport is obtained for BGSD and SGM when the gates are closer to the drain contact, resulting in shorter transit times and longer free flights.

3. Conclusions

The influence of gate misalignment on the static characteristics of DG-SB-MOSFETs was determined carrying out systematic simulations with the Monte Carlo method according to three ideal misalignment scenarios. Static characteristics proved to be highly sensitive to gate misalignment specially compared to traditional MOSFETs. The changes in the concentration profile due to the modification of the quantum tunneling injection process provoked by gate variability has been found to play the major role.

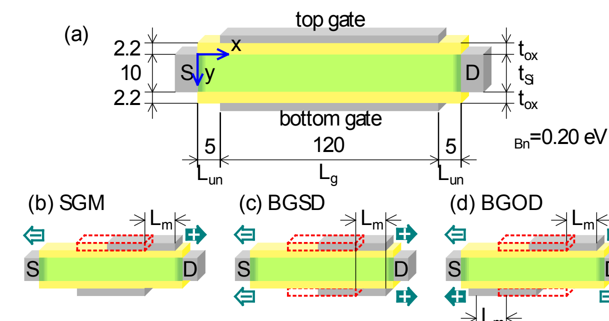

Fig. 1. (a) Device topology and (b, c, d) simulated double gate misalignment scenarios (dimensions in nm)

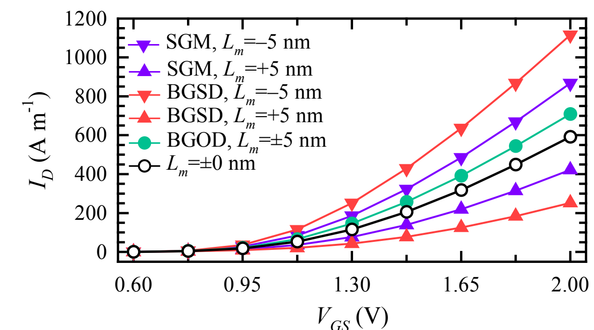

Fig. 2. Drain current vs. gate voltage curves for the extreme missalignment values on the three scenarios with V_{DS}=2.0 V

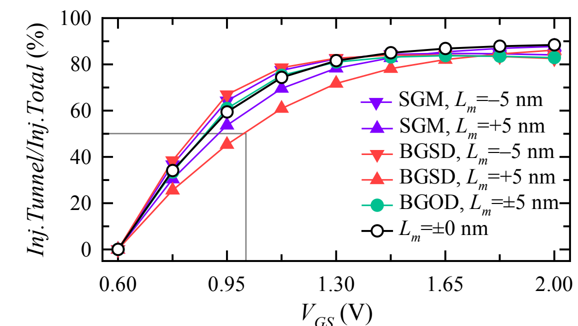

Fig. 3. Injected tunnel current/total injected current ratio for the three scenarios and extreme misalignments as a function of V_{GS} for V_{DS}=2.0 V

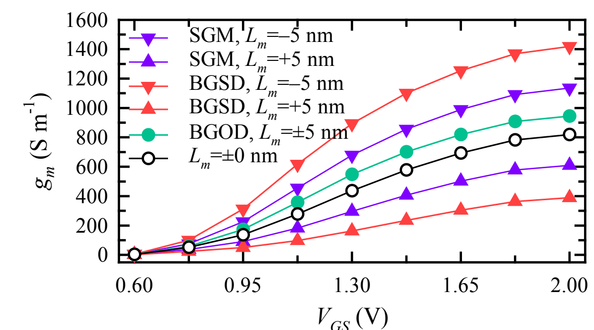

Fig. 4. Transconductance for the ideal device and the extreme L_m values for every scenario with V_{DS}=2.0 V

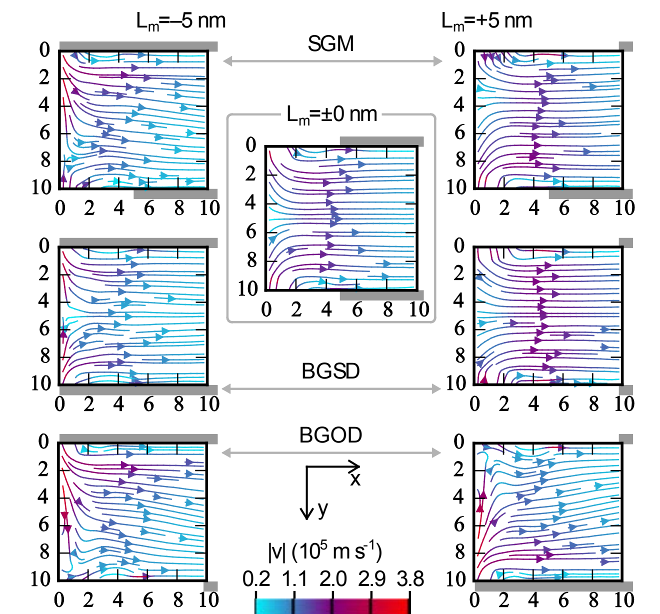

Fig. 5. Carrier motion and speed in the vicinities of the source contact for the three scenarios and the extreme misalignments when V_{GS}=V_{DS}=2.0 V. Gray rectangular shapes represent gate positions for each case

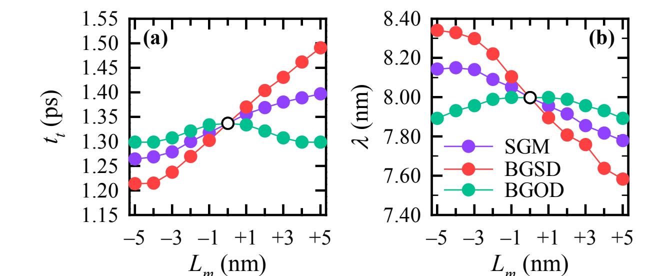

Fig. 6. (a) Mean carrier transit time, tt and (b) free flight distance, λ for V_{GS}=V_{DS}=2.0 V

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Design of an enhanced MEIGA-MetNet dust micro-sensor able to perform gas sensing in Mars atmosphere

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Mars MetNet Mission was born as a collaborative project that involves Finland, Russia and Spain researchers, with the aim of providing a network formed by several tens of atmospheric stations along the Martian surface [1]. MEIGA-MetNet payload is the Spanish contribution to this mission, where an extensive atmospheric science payload onboard a landing vehicle with strong weight and power budgets (45 g and 1 W). Infrared Laboratory from Universidad Carlos III de Madrid (LIR-UC3M) has faced the design and development of a micro-sensor, based on infrared (IR) detection principles, both scattering and absorption, focused on dust characterization in terms of the particle size distribution, carbon dioxide concentration and temperature [1].

In the framework of MEIGA-MetNet project, LIR-UC3M has approached this challenge through the development of radiative transference models in order to establish proper design criteria [2]: spectral selection, source-detector geometric configuration, data retrieval algorithms and finally the optimization of the dust sensor (DS) performances.

It is well known from both in-situ and remote sensing measurements that the main compound of Martian aerosol is micron-sized dust coming from soil. Its density and size distributions influence the thermal behavior of the lower atmosphere by absorbing or scattering solar radiation processes [3]. Therefore, dust suspended in the atmosphere is a major agent of atmospheric motions at all scales and has a great influence on the morphological evolution of the Martian surface [2] and its planetary boundary layer (PBL).

Otherwise, in addition to suspended dust there exist other parameters that greatly contribute to the knowledge about Martian atmosphere and climate. For instance, the presence of carbon dioxide (CO_2) in the Mars atmosphere has a big influence on weather, while its concentration is strongly affected by temperature cycles through condensation and sublimation processes [4]. CO_2 is the major concentration compound in Martian atmosphere and consequently the main vector for transportation of the rest of atmospheric compounds. These phenomena involve the transportation of large amounts of the rest of atmospheric compounds. Water vapor concentration, for instance, suffers from a big variability induced by the one of CO_2 [4]. H_2O vapor is one of the most significant compounds of Martian atmosphere. Its measurement is not only important for a better understanding of the PBL processes but also for future manned missions, as they can show where important ice reservoirs might be located.

In addition, Carbon Monoxide (CO) is another compound present in Martian atmosphere. Although its presence is not as significant as CO_2 and water, as in the case of methane, it may reveal evidence of geological activity or clarify about biologic origin or not of some compounds.

In this context, the proposed work addresses the enhancement of the current version of the dust sensor, by providing gas sensing features for CO_2, CO and water vapor compounds. Other compounds like methane could be addressed in future upgrades of the sensor as they can be detected by similar principia.

For these purposes, a full radiometric model (including source, detector, optics and spectroscopic databases) has been built as a tool for system design and simulations.

Finally, a new gas sensing system design is proposed where the most relevant specifications as detection limits and uncertainties are estimated through software modeling. Moreover, an initial design has been carried out in a breadboard model of the micro-sensor.

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